DesignCon 2022

On-chip ESD Protection Structure Modeling Methodology

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Abstract

Electrostatic discharge (ESD) events can result in soft and hard failures to an integrated circuit (IC). To protect the ICs from ESD, ESD protection structure is critical for chip-level design. Since chip-level internal ESD protection circuit information is often not released to the public, we propose a new modeling methodology using vector network analyzer (VNA), time domain reflectometer (TDR), source meter unit (SMU), and three-terminal transmission line pulse (TLP) test, for the first time, to accurately obtain both quasi-static current-voltage (IV)-curves and small signal model of the on-chip ESD protection structure based on the published single Transient Voltage Suppressor (TVS) modeling framework. Besides, the transient waveform characterization using very fast TLP (VF-TLP) for discrete on-chip ESD protection structure is investigated and an improved modeling methodology is proposed. Our proposed measurement-based IC ESD protection modeling is verified by simulation and measurement results on multiple ICs. Our proposed model can be further used in optimizing the system-level ESD protection without information on internal IC ESD protection scheme.

Authors' Biography

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Introduction

Information on on-chip ESD protection structures on ICs are often not available to the public. No modeling framework has been proposed to reveal the detailed information on internal ESD protection schemes on different IC pins accurately. A typical on-chip ESD protection structure for signal pin consists of a dual diode and power rail clamp [1]. The characterization method for individual dual diode structure and individual power rail clamp has already been published [2]. However, with the increasing requirement of the on-chip ESD protection, the protection structures are usually combined inside the chip, which dramatically increases the complexity and uncertainty of characterizing each ESD protection structure individually. Although a simplified characterization method, which considers the structure as a single TVS structure, on IC pins may provide some level of information to allow protection for low ESD stress, it can also lead to larger discrepancy at higher ESD discharge output. Unlike the internal chip-level ESD protection structure for general input/output (IO) ports, other IOs, such as radio frequency (RF) IO and power rails, have different internal chip-level ESD protection structures which require a new methodology to characterize the behavior model to satisfy the system level analysis requirement.

The small signal and the large signal model must be both considered for accurate characterization of the internal ESD protection. A systematic modeling approach using VNA, TDR, SMU and TLP measurement is used to extract small and large signal model. A three-terminal measurement-based modeling is used to extract quasi-static IV curves for each ESD protection component inside the IC without additional access to the internal structure of the IC.

This paper consists of analysis on self-designed evaluation fixture for various on-chip ESD protection structures, including two-terminal diode structure, three-terminal diode structure, discrete power rail RC-triggered clamp and discrete inductor under no DC power input. Our proposed measurement-based internal IC ESD protection modeling also shows good correlation between simulation and measurement.

This paper presents the most accurate internal IC ESD protection modeling methodology to improve system-level ESD design modeling techniques without the prior knowledge on internal structure of the ICs.

Overview of Single TVS Modeling Methodology

A TVS transient behavior characterization and the corresponding SPICE-based behavior model [3] has already been modeled for a single TVS, as one of the ESD protection components. Based on this model, different types of ESD protection components, such as snapback TVS, non-snapback TVS, varistor and spark gap like device, have been tested and validated using the TVS model and applied to the System Efficient ESD Design (SEED) simulation [4]. The model can be divided into two parts, the small signal part and the large signal part, as shown in Fig. 1. For small signal part, the required known information for the model is the parasitic inductance, the parasitic capacitance and the resonance impedance. For large signal part, the modules are all behavior-based model and are separated according to the functionality. The large signal part is designed to meet the requirement of quasi-static IV curve fitting and the transient response.

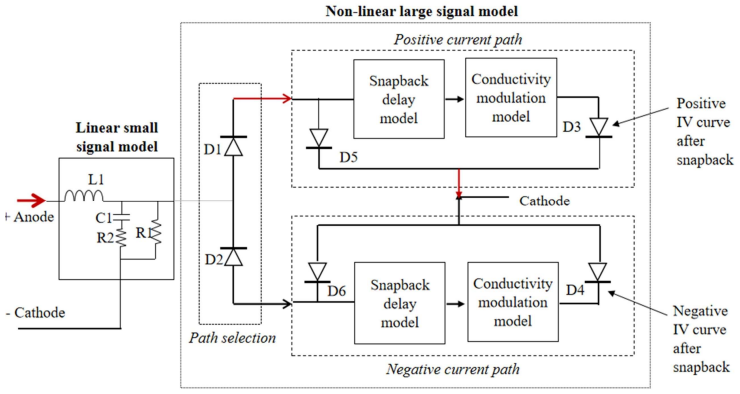
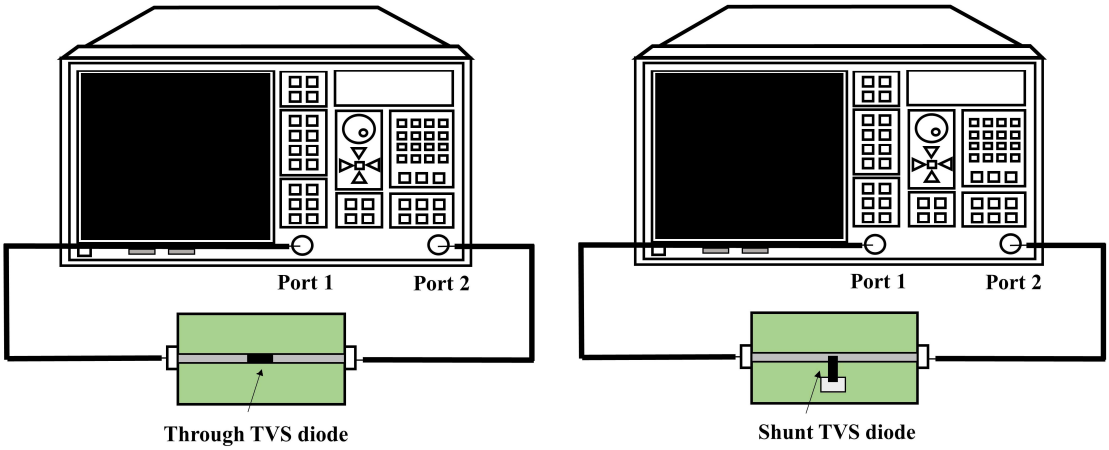


Fig 1. TVS modeling framework

Small signal part is considered as a linear sub-part, which means that the interaction between each component within the block should not affect the measured result of individual components. Using VNA and TDR, individual components can be separately characterized. On the other hand, the large signal sub-part, due to the nonlinear behavior of the quasi-static voltage and current waveform and the multi-factor influence to the first few nano-second response, should be characterized in time domain. Therefore, TLP test is designed to characterize the quasi-static IV curve and VF-TLP, which utilizes the theory of TDR, is designed to characterize the transient response.

A. Small Signal

To characterize the small signal sub-part, the device under test must be mounted on a 50 ohm evaluation fixture. In Fig. 2, a TVS diode is used as an example DUT. To measure the parasitic capacitance and inductance of the diode, two different setups are required [5]. Frist setup is a through structure, to measure the S_{21} to extract the parasitic capacitance, as shown in Fig. 2(a). The second setup connects the diode in shunt structure to extract the parasitic inductance and the resistance at the resonance point, as shown in Fig. 2(b).



(a) TVS DUT in series to a through-fixture. (b) TVS DUT in shunt with test fixture.

Fig 2. VNA setup to measure the small signal components

The measured capacitance is calculated by:

$$C_1 = \left|\frac{S_{21}}{j2\pi f[100*(1-S_{21})]}\right| \tag{1}$$

where S_{21} is the complex-numbered measured result and f is the selected measured frequency.

The measured inductance is calculated by:

$$L_1 = \frac{1}{4\pi^2 {f_0}^2 C_1} \tag{2}$$

where C_1 is the calculated parasitic capacitance and f_0 is the resonance frequency.

The measured resistance at the resonance frequency is calculated by:

$$R_2 = \left|\frac{25*S_{21}}{1-S_{21}}\right| \tag{3}$$

The R_1 shown in Fig. 1 represents the leakage resistance of the TVS diode, which is relatively larger in the order of 1 MOhm, and can be ignored for the TLP test.

B. Large Signal

There are four sub-modules that need to be modeled for large signal sub-part. Depending on the different targets, the model requires both standard TLP test and very fast TLP test to model different modules [3]. They are divided into different categories by different TLP tests.

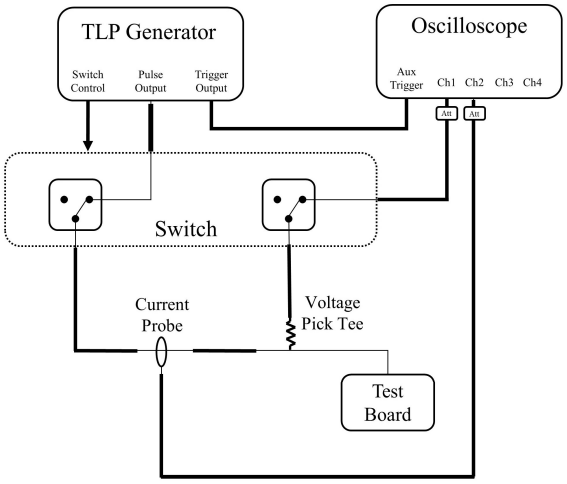


Fig 3. Standard TLP setup diagram

1) **Standard TLP test:** Standard TLP test setup is shown in Fig. 3. TLP generator generates a square wave with 100 ns pulse width to the test board with IC under test. The 100 ns pulse length ensures that the voltage and current measured will eventually reach a stable level. For the setup used in this paper, the stable region window is 70ns~90ns and the average voltage and current within this 20 ns is the quasi-static voltage and current for applied discharged voltage level of TLP generator. The IV curve can be used to model diodes, D3 and D4, shown in Fig.1. The current measurement is done by the current probe, CT-1, which can work up to 1 GHz. The voltage measurement is done by a voltage pickup tee, which uses 1-kohm as the pickup resistor.

The calculation for the real current waveform is:

$$I(t) = \frac{V_{osc\_ch2\_50oh}\ (t)}{k} \tag{4}$$

where $V_{osc\_ch2\_50oh}\ (t)$ is the measured waveform of channel 2 on the oscilloscope when the channel is terminated with 50 ohm and k is the calculation coefficient of the CT-1 probe, which was 5 for the CT-1 probe used in the setup.

The calculation for the real voltage waveform is:

$$V(t) = \frac{R_{pickup}+R_{50oh}}{R_{50oh}} * V_{osc\_ch1\_50ohm}(t) \tag{5}$$

where R_{pickup} is the pickup resistor, 1 kohm, and R_{50ohm} is the 50 ohm termination of the oscilloscope, and $V_{osc\_ch1\_50ohm}(t)$ is the measured waveform of channel 1 on the oscilloscope when the channel is terminated with 50 ohm.

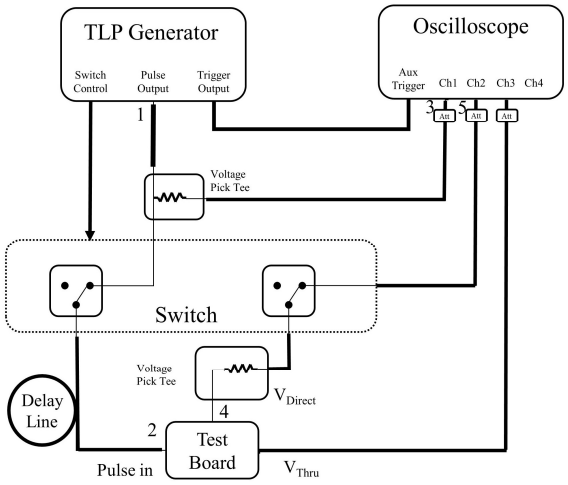


Fig 4. VF-TLP setup diagram

2) Very Fast TLP Test: The measurement setup is similar to the standard TLP test, as shown in Fig. 4, but they have fundamental differences. In standard TLP test, there is some physical distance from the voltage and current measurement location to the IC pin of the device, because of finite physical size of probes introduced into the measurement setup inevitably. Such small physical length difference can be ignored for quasi-static IV curve because the physical length has negligible impact on the measured result during 70%~90% time window after the arrival of TLP. However, the first few nanoseconds after the arrival of the TLP is critical for characterization of conductivity modulation and snapback delay module shown in Fig. 1.

Very fast TLP (VF-TLP) uses fast rise time and short pulse to characterize the exact transient response by post processing to separate incident waveform and reflected waveform, which are distinctively separated by a long delay transmission line. For the voltage measurement, the pickup tee can be directly soldered at the pin of the device on the evaluation board. The voltage waveform is again calculated using (5). For the current waveform, additional measured voltage waveform is needed, located far away from the test pin. A simplified circuit for the TDR measurement is shown in Fig. 5. Another voltage pick tee is placed at this additional far distance measurement point with sufficient delay to distinguish incident and reflected voltage. For example, the measured voltage waveform in channel 1 of the oscilloscope will be similar to the one shown in Fig. 6.

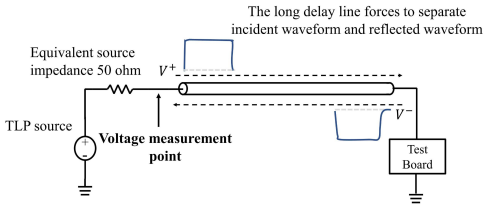


Fig 5. Simplified circuit for TDR measurement, long delay line will separate the incident waveform and reflected waveform

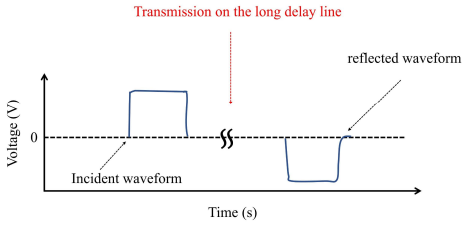


Fig 6. Measured time domain waveform

The post-processed current waveform can be calculated as:

$$I(t) = I_{inc} + I_{ref} = \frac{V_{inc} - V_{ref}}{50} \tag{6}$$

where V_{inc} is the measured incident waveform and V_{ref} is the measured reflected waveform.

Once the incident waveform and the reflected waveform has been separated, the waveform can then be post-processed to be compensated for the added delay and (6) can be used.

However, VF-TLP requires more precise result to improve the transient modeling. The long delay line and the measurement cables will cause non-negligible impact to the loss. The measured data needs to be processed in frequency domain and use several S_{21} results of the signal transmission path to compensate the loss [6].

In reference to the node numbers in Fig. 4, for the voltage waveform, the result should be translated back from node 5 to node 4, which means the measured voltage spectrum must be divided by S_{45}, transfer function between node 4 and 5. For the current waveform, incident waveform and reflected waveform must be post-processed separately.

First, for incident waveform, the measured waveform is post-processed back from node 3 to node 1, which is the TLP output. As next step, the waveform is post-processed again from node 1 to node 2, at the test board. In summary, the waveform is divided by S_{13}, the transfer function between node 1 and 3 followed by multiply S_{21}, the transfer function between node 2 and 1.

Second, for the reflected waveform, the measured waveform only needs to be post-processed from node 3 to node 2, that is, be divided by S_{23}, transfer function between node 2 and 3.

The final voltage and current waveform after loss compensation is calculated as:

$$V(t) = iFFT\left[\frac{FFT\left(V_{osc\_ch2\_50ohm}(t)\right)}{S_{45}}\right] \tag{7}$$

$$I(t) = \frac{iFFT\left[FFT\left(V_{inc}(t)\right) * \frac{S_{21}}{S_{13}}\right] - iFFT\left[\frac{FFT\left(V_{ref}(t)\right)}{S_{23}}\right]}{50} \tag{8}$$

Once the small signal data, the quasi-static IV and the transient waveform is available, the TVS can be modeled following the modeling steps in [3]. The model is verified to be accurate and can be applied to SEED simulation.

On-chip ESD Protection Structure Categories and Modeling Methodology Evaluation

The devices for on-chip ESD protection include: Diode, NMOS and Silicon-controlled Rectifier (SCR). Generally, diodes and SCR can both be modeled using the TVS model, thus in the modeling TVS model is used to characterize all the diode structure and SCR structure.

Three types of ESD protection structures are under investigation: Normal IO, power rail and RF IO. Through out the paper VDD refers to the DC power and VSS refers to the ground terminal.

1. Normal IO contains the peripheral IOs used for general purposes, such as GPIO and USB.
2. Power rail is designed for DC voltage input, therefore the ESD protection structure for power rail should be able to distinguish the ESD stress and from the power-on DC voltage.
3. RF IO has a target signal frequency range. This requirement limits the choice for ESD protection on RF IOs. Regular diodes are not suitable because of parasitic capacitance. So different ESD protection strategies are often used for RF IO.

For each type of IO, a typical or anticipated ESD protection structure is depicted in Fig. 7. In each of the following sub-chapter, detailed analysis and evaluation for each IO are provided.

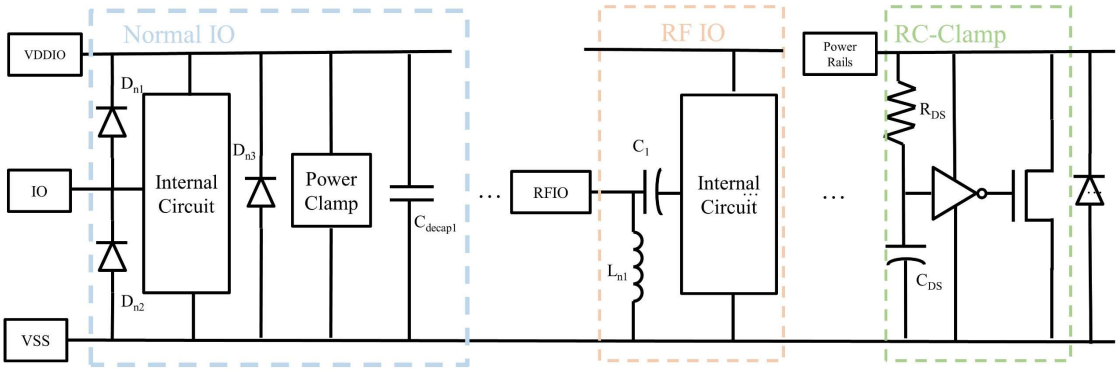


Fig 7. Proposed general ESD protection structure design for normal IO, RF IO and power rails.

A. Normal IO

Normal IO refers to peripheral IOs that do not have any specific operating frequency. Therefore, widely known ESD projection scheme using diode structure is commonly used . Typical ESD protection structure using diode contains VSS-based and VDD-based diode structure [7].

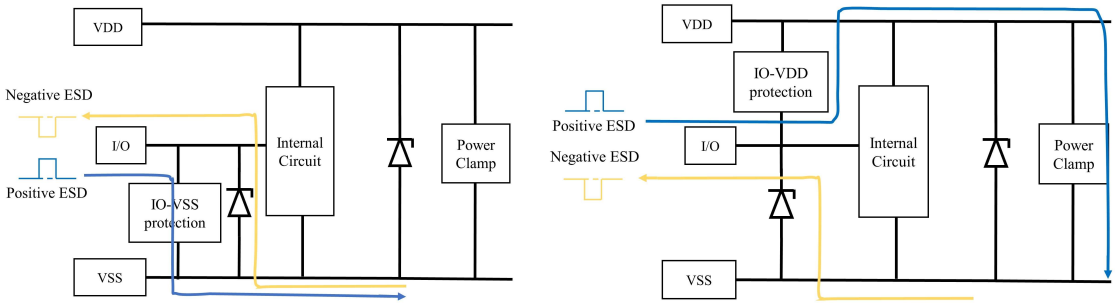
1) VSS-based structure

VSS-based structure has one ESD protection structure connected from IO to VSS to shunt current to VSS rail, adding another diode in parallel to conduct negative

ESD pulse, as shown in Fig. 8(a). This structure can be simplified as a unidirectional TVS diode.

2) VDD-based structure

VDD-based structure has one ESD protection structure connected from IO to VDD, to guide positive ESD pulse to the power rail and then discharges through the power clamp to VSS, while there is still another diode from IO to VSS to conduct negative ESD pulse, as shown in Fig. 8(b). This type of structure can be modeled as a three-terminal diode structure.



(a) VSS-based ESD protection structure (b) VDD-based ESD protection structure

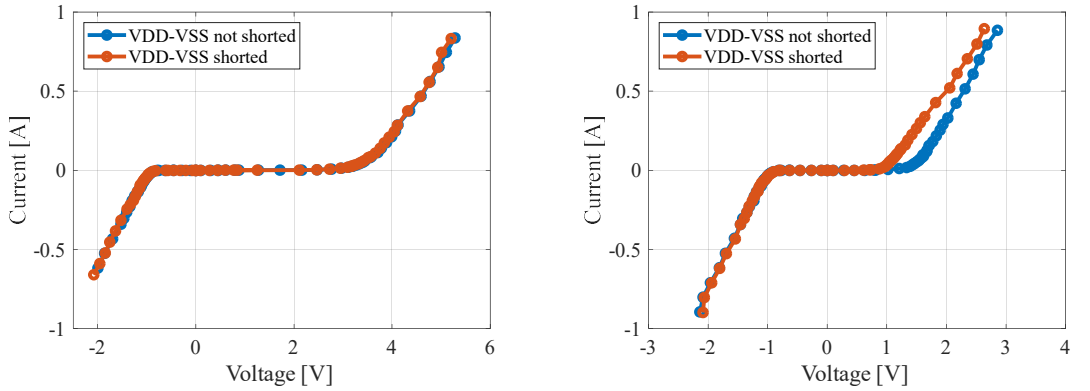
Fig 8. VSS-based and VDD-based ESD protection structure. (a) IO-VSS protection and the parallel diode can be combined as one diode. (b) IO-VDD protection, IO-VSS clamp and VDD-VSS clamp is considered as a three-terminal structure

For VSS-based structure, a standard TLP test can be used with no DC power to show the effect to the IO-VSS diode characterization caused by the power clamp in Fig. 9(a). The only difference between two curves shown in Fig. 9(a) is whether VDD and VSS are shorted or not. Both the IV curve and transient waveform show almost no change when VDD-VSS is shorted. Therefore, for this specific pin, the measurement result has verified that that the unidirectional TVS diode modeling can be separately characterized with negligible effect from the power clamp. The same conclusion can be made to the power clamp characterization under VSS-based design concept. Thus, for VSS-based structure, the modeling characterization methodology introduced in single TVS modeling methodology can be directly applied with acceptable discrepancy.

For VDD-based structure, the same TLP test setup is used. The measured IV curve is shown in Fig.9(b). The modeling method needs to be different from the case of Fig. 9(a) because the IO-VDD ESD protection provides another path for ESD stress to the power rail and return to VSS via power clamp. When the I/O pin is injected with a positive mode ESD stress, a portion of ESD current must be discharged to ground through a diode and a power clamp with some additional portion through the IO-VSS diode. Due to the limited accessibility to the internal structures of the IC, it is difficult for hardware designers to separate the shared current in two different paths. The measured transient waveform and small signal model also require improved modeling methodologies, which will be introduced in the next section.

VDD-VSS diode is a simplified equivalent model to describe the combination of both the power clamp with and without another TVS diode, depending on the IC pin. The

working condition of power clamp is different from TVS diode [8]. Therefore, to separately characterize them, more information about the internal protection design inside the chip is necessary. However, for a hardware designer VDD-VSS diode model can be sufficient for ESD protection analysis.



(a) TLP test on IO port for VSS-based structure (b) TLP test on IO port for VDD-based structure

Fig 9. The difference of TLP tested IV curves on IO port, (a) for VSS-based structure, the power clamp almost has no effect to IO port characterization, (b) for VDD-based structure, the power clamp will contribute to the turn on voltage shift and dynamic resistance change

B. RF IO

Most of ESD protection scheme will lead to additional parasitic capacitance when used on RF signal pins. The parasitic capacitance can change the signal bandwidth and may result in distortion and signal degradation. Therefore, some IC vendors strategically utilize the STI diode with low parasitic capacitance compared to a gated diode for RF IO ESD protection [9]. Another effective ESD protection method for RF IO is to directly use inductors as the ESD protection device for RF IO. Inductor guides the ESD current (low frequency) away and blocks the RF signal (high frequency). This inductor should be in the low nano-Henry range (<20 nH) to be an effective ESD protective solution [10].

Possible ESD protection structure of the RF IO is shown in Fig. 7, the capacitor is used to pass the RF signal and block the ESD current. Therefore, only one additional inductor and the corresponding series resistance need to be characterized when using inductor as the ESD protection. For RF IO with ESD protection with diode, previously proposed TVS modeling methodology to characterize the ESD protection structure.

During the characterization, a multi-meter can be used to check the DC resistance from the RF IO to VSS for identification of type of the RF IO ESD protection. RF IO ESD protection scheme with an inductor will show low-value resistance using a multi-meter, while RF IO ESD protection scheme with diode will acts as an open termination in reverse bias mode.

Once the multi-meter results verifies that the RF IO ESD protection scheme uses an inductor, 1-port VNA measurement with port extension and loss compensation can be used to obtain the inductance value. According to the reference of Keysight E5071C, used in our verification, two measured points can be used when calibration to get a fitted loss

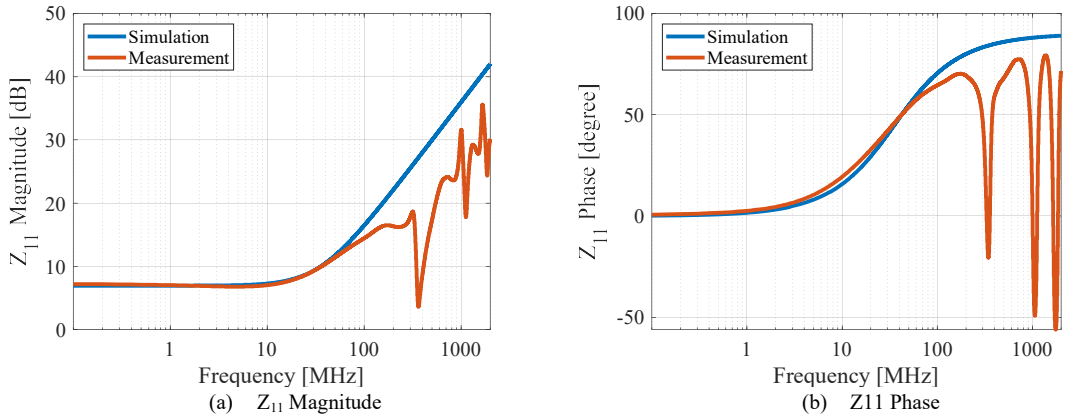
function curve defined as:

$$Loss(f) = Loss_1 * (\frac{f}{Freq_1})^n \quad (9)$$

where n is calculated as:

$$n = \frac{\log_{10} |\frac{Loss_1}{Loss_2}|}{\log_{10} \frac{Freq_1}{Freq_2}}$$

The final post-processed measurement result for RF-IO pin example and the circuit simulation using the obtained inductance value validates good correction on magnitude and phase up to 50 MHz, as shown in Fig. 10. Since inductance and the series resistance are only dominant at low frequency below 50 MHz, correlation at frequencies beyond 50 MHz is not necessary.



(a) Z_{11} Magnitude (b) Z11 Phase

Fig 10. Final characterized result and the simulation validation on (a) Z_{11} magnitude and (b) Z_{11} phase. The inductance is 10nH and the series resistance is 2.23 Ohm.

C. Power rail

A power clamping structure is commonly used to protect ICs against power bus ESD surges.

- Multiple finger gCNMOS(Gate-Coupled NMOS) and SCR type structures are good candidates for power clamps [2].
- Another proven power clamp is based on a forward diode string or Darlington [2].
- Big-NMOS based power clamp also works [11].

Among all the different structures of power clamp, big-NMOS with RC-triggered clamp is the most general choice. RC filter helps to distinguish the response to ESD stress whether to switch on the inverter and the big-MOS to conduct the ESD current to ground. When there is no ESD stress, the inverter is always off because RC-triggered clamp is not

triggered, and the power can normally supply the working circuit from VDD to VSS.

To design suitable RC-based circuit, the RC time constant must be designed about 1 microsecond to trigger the clamp and keep it in a conducting state for the entire duration of the ESD event which is approximately 600–750 ns for the HBM ESD stress. To satisfy this specification, R is typically realized with a 50 kΩ n-well resistance and C is realized with a 20 pF poly-gate of NMOS transistor. Large resistance and capacitance needed for the time constant occupies a large silicon area [12].

For RC-clamp characterization, the components can be characterized simply by using TLP and recording the time domain waveform [8]. However, for any of IC protection characterization, the internal circuit as well as the parasitic components influence the transient time domain waveform. Hence, simple TLP test is not an option. However, the behavior of the RC-triggered clamp is mostly based on the big-NMOS operation, the IV-curve will show small snapback behavior and turn on at a low clamping voltage due to the thin gate oxides and the gate-coupled structure [7], which means the characterization of the RC-triggered clamp can be similar to the general TVS diode. The key challenge here is to identify the working condition of the clamp under ESD stress. This can be done by comparing SMU and TLP measurement result.

The SMU used in the measurement is Keithley 2401. There are two key differences between SMU and TLP:

- Pulse width. TLP will generate the pulse with around 100 ns pulse width while SMU provides milli-second pulse or even longer. SMU is limited to a relatively low current level, usually in the order of 1mA, but it is often sufficient to observe the ESD protection structures' turn on behavior.
- Rise time. TLP's rise time is usually set to be around 1ns. It can be adjusted to be faster or slower according to the different analysis targets. SMU's rise time, on the other hand, is much slower than TLP, usually in the order of micro-seconds.

By connecting SMU and TLP to the power rail, the rise time difference in two equipment helps determine whether RC-triggered clamp exists in our RF-IO ESD protection or not. The designed RC filter inside the trigger clamp could easily distinguish the ESD pulse rising edge and turn on the big NMOS to divert the ESD pulse from power rail to VSS rail ,as shown in Fig. 11. If no RC triggered clamp exists, the ESD pulse will either pass through the dual diode structure, the reverse diode from VDD to VSS or through the on-chip decoupling capacitor, and all possible discharge paths will provide a different result from the RC-triggered clamp,

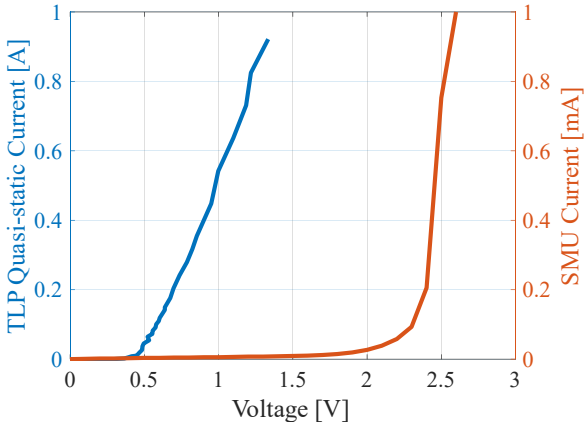


Fig 11. Measured IV curve comparison on RC-Triggered clamp between SMU and TLP. The RC-Triggered clamp will turn on at relatively low voltage when using TLP, but it won't turn on when using SMU. For SMU test, ESD stress passes through other structures instead of RC-triggered clamp

Without having access to inner pins, it is challenging to characterize the exact RC time constant, the inverter and the big-NMOS inside the IC. Besides, the improved structures, such as booster rail and on-time control circuits, for trigger clamp can distinctively change the characterization result, which makes the problem more challenging. However, the method could help distinguish the structure used for power rail ESD protection, such as the grounded-gate NMOS structure or the Darlington diode. For RC-triggered clamp, during the ESD event, the characterization result based on the single TVS model still shows a good performance.

Three-terminal modeling methodology

Among all different types of IC ESD protection structures, the three diodes structure modeling is most complex and time consuming. The interaction among the three diodes causes the non-linear combination in large signal part. Different injection points and changing return paths can provide more analytical equations to solve the non-linearity, but there are other disadvantages include:

1. The characterization method requires more measurement cases and additional manually fitting optimization
2. The modeled structure is not verified to be true at higher ESD discharge levels.

To accurately characterize the three-terminal model, there are several published papers based on the simplified model. One three-terminal modeling methodology in [13] only uses the quasi-static IV model without considering the power rail difference, the parallel RF components and the transient response. Another attempt in [14] for three-terminal modeling takes the on-chip components into consideration and provides the extraction in detail, while it still lacks the full modeling process according to the single TVS model.

However, the characterization methodology requires not only the quasi-static IV but also the small signal and the transient response. Hence, an improved three-terminal

modeling methodology is proposed. An IO on an IC with three-terminal ESD protection structure is used to evaluate the corresponding modeling methodology, as shown in Fig. 12. In measurement, the measured result will inevitably involve the capacitance and inductance from the internal circuit, such as the on-chip decoupling capacitor, other filter components, and the loop inductance. Thus, here we use equivalent components, such as parallel capacitance instead of parasitic capacitance, to describe the total measured parameters. To show the characterization procedure, a real IC is used to provide clear modeling results.

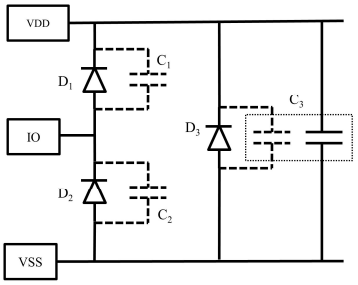


Fig 12. Parallel capacitance schematic for different diodes.

A. Parallel Capacitance

To characterize the small signal model of the three-diode structure, the main dominated part would be the characterized capacitance. For inductance, the characterization method is mostly based on the transient waveform, thus only the inductance will be left in large signal measurement to characterize.

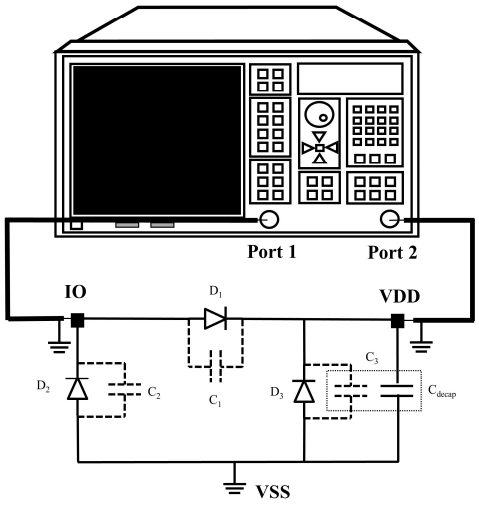


Fig 13. 2-port VNA measurement setup to extract C_1, C_2 and C_3

The capacitance is generally connected in three-terminal structure as well, so in frequency domain measurement, the result is linear and time-invariant, and can be separately calculated. By connecting the whole three-terminal network to the VNA using two port measurement, from IO port to VDD port, we can measure the whole S-parameter of the network, as shown in Fig. 13. Only consider the capacitance dominated frequency

band (from 1MHz to 10MHz) and simplify the circuit to a capacitor lossless π-network, as shown in Fig. 14, the whole network can be calculated out through π equivalent circuit for admittance parameter [15].

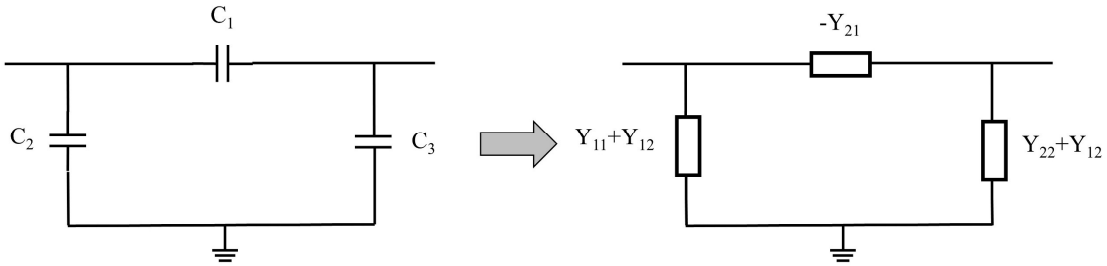


Fig 14. The circuit is simplified to be purely imaginary. Use Y parameter(admittance parameter) to calculate π equivalent circuit.

C_1 can be calculated as:

$$C_1 = \left|\frac{-Y_{21}}{2\pi f}\right| \tag{10}$$

C_3 can be calculated as:

$$C_3 = \left|\frac{Y_{22}+Y_{21}}{2\pi}\right| \tag{11}$$

where f is the corresponding selected frequency at 20dB/dec region between 1MHz and 10MHz.

During the VNA measurement, some of the IOs may contains internal diode inside the internal circuit, which will unexpectedly turn on if the VNA output power is higher than the V_T of the diode. To avoid such condition, lower power level is suggested for all the VNA test. A suggested value is -10dBm, which is roughly 0.1V for the peak of the output signal.

However, due to the limitation of the accuracy for S_{11} measurement in VNA for small capacitance(a few pF or below), though C_2 can still be calculated using the admittance parameter, the accuracy of the result for C_2 cannot be guaranteed. Therefore, capacitance measurement using TDR is introduced to compensate for the inaccuracy of the C_2 result.

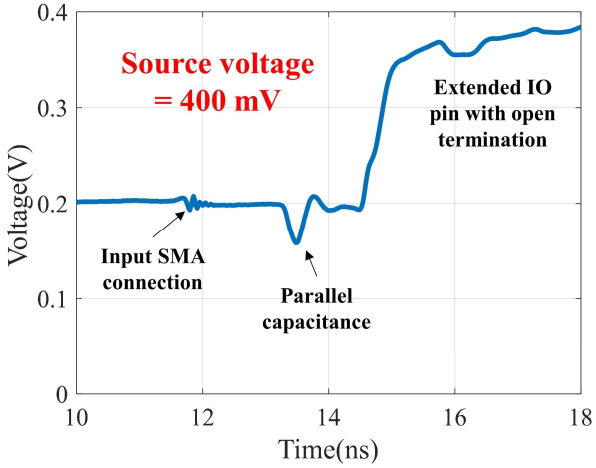


Fig 15. TDR measurement result at IO port, the middle parallel capacitance region is the calculation region

As shown in Fig. 15, the measurement TDR result at IO port shows three apparent changes. The middle one is the parallel capacitance change. By applying the capacitance calculation equation to the shunt capacitance using TDR [16] we have:

$$C_{TDR} = -\frac{2}{Z_0}\int \frac{reflect(t)}{incident\_ht}dt \tag{12}$$

where Z_0 is the characteristic impedance of the trace; $reflect(t)$ is the reflection waveform, it can be obtained by using measured TDR waveform, which is measured when TDR is connected the IO, to subtract the normal TDR waveform, which is measured when TDR is connected to open. $incident\_ht$ is the height of the incident waveform, here the value is 400mV

While by connecting the TDR port to IO port, the measured capacitance is not any of the single capacitance, but a combination of the three capacitances:

$$C_{TDR} = C_2 + \frac{C_1 C_3}{C_1 + C_3} \tag{13}$$

By applying the measured C_1 and C_3, we have the calculated C_2

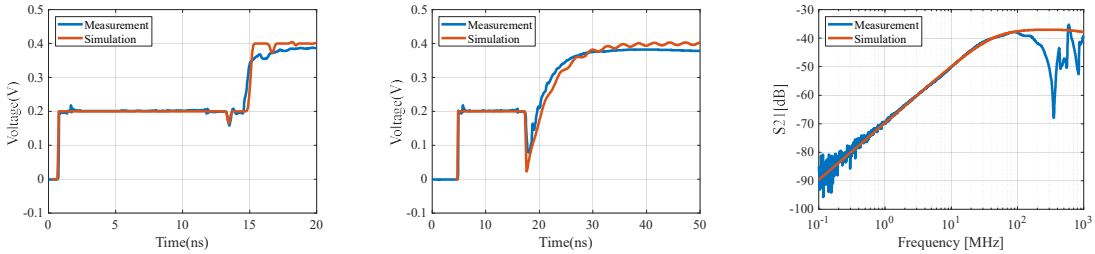
$$C_2 = C_{TDR} - \frac{C_1 C_3}{C_1 + C_3} \tag{14}$$

TDR can also be used to mainly validate the measured C_3 by connecting the TDR port to VDD port. The rise time is determined by the rising time from 0 to $0.632V_{max}$, while it also refers to the characteristic impedance times the capacitance. Therefore, by using TDR on VDD port result, it can be calculated as:

$$\tau = Z_0\left(C_3 + \frac{C_1 C_2}{C_1 + C_2}\right) = t_{0\sim 0.632V_{max}} \tag{15}$$

where $t_{0\sim 0.632V_{max}}$ is the time length of the waveform rising from 0 to 0.632*maximum TDR voltage.

To achieve the most accurate result, VNA measurement is used to characterize C_1 and TDR measurement is used to on both IO port and VDD port. Equation (10), (14) and (15) are used to calculate out C_2 and C_3. The measurement and validation results are shown in Fig. 16.



(a) TDR result on IO port (b) TDR result on VDD port (c) VNA 2-port test result

Fig 16. The measurement and validation result for (a) TDR test on IO port (b) TDR test on VDD port and (c) VNA 2-port test. The calculated result is C_1=0.52pF, C_1=1.17pF, C_1=71.04pF

B. Quasi-static IV curve

The main issue to be solved in quasi-static IV curve characterization is how to separate the current through D_2 from the measured current at IO port. Whether the ESD stress discharges to IO or VDD, whether the ESD stress is positive or negative, the different

discharge paths will share the measured current. And from the general single TVS modeling, it's clear that the IV-curve modeling of each TVS diode is time-variant and voltage-dependent. This implies a non-linear characterization problem on large signal modeling. The modeling requires external operations to de-embed one diode from another during standard TLP test. Only three pins, which are VDD, VSS and IO, are available for characterization. In order to separately model each diode, the target would be extracting the separated voltage across each single diode and the separated current through each single diode. The whole process is concluded in flow chart as shown in Fig. 17.

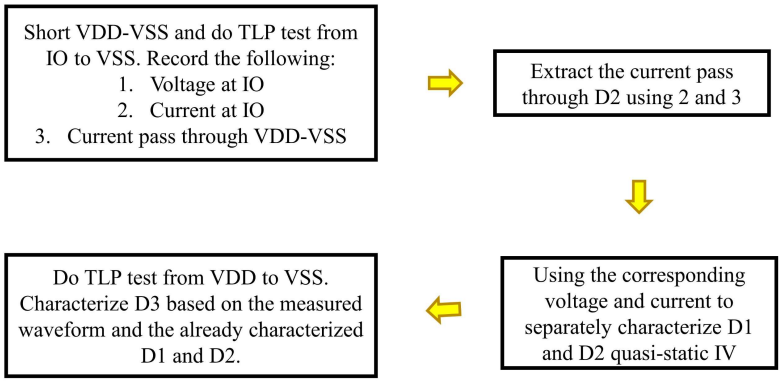


Fig 17. Flow chart for three-terminal quasi-static IV curve extraction

1) To reduce the complexity of the three-terminal structure, the first step is to manually remove one diode from the structure. A simple way is to short the diode, for example, short VDD to VSS at power off case to remove the effect caused by D_3. This method will inevitably introduce some inductance, but this could be modeled during SPICE tuning.
2) The second step is to separate the current through D_1 from the measured current at IO. Though there is no access to D_1 from IO to VDD, it's clear that VDD has been shorted to VSS thus all the discharge current on IO to VDD path will be shunt through the short circuit. According to the feature of the current probe that the path through the probe is an equivalent short circuit, a current probe can be used on the shorted VDD-VSS circuit, as shown in Fig. 18. The current measured is the current through D_1 and the current through D_2 can be extracted by subtracting the D_1 current from the measured current at IO.

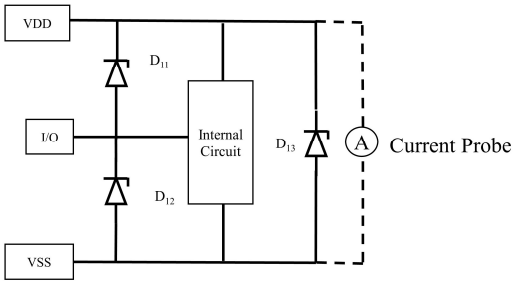


Fig 18. Using current probe to short VDD to VSS

3) Once the current through D_1 and D_2 extracted, the voltage measured at the IO is exactly the voltage across D_1 and D_2 and can be directly used for quasi-static IV modeling. An example is provided for TLP output equals to 10V in Fig. 19

according to the subtraction. Though the first few nanoseconds may not be accurate, the 70%~90% region will reach the stable level, which means it can become the window for quasi-static IV curve characterization. The final extracted quasi-static IV curve is shown in Fig. 20. It can be directly used to characterize the diode after snapback shown in the single TVS model in Fig. 1.

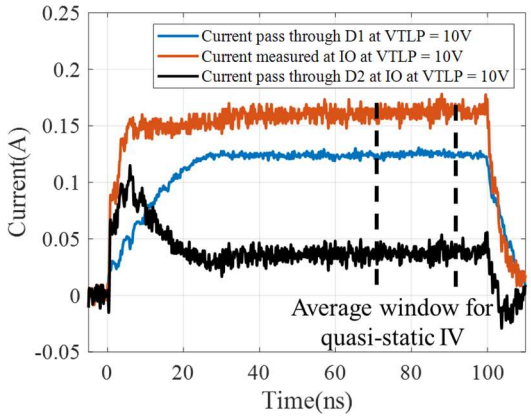


Fig 19. Subtraction process to obtain the current pass through D_2, the different at first few nanoseconds can be ignored.

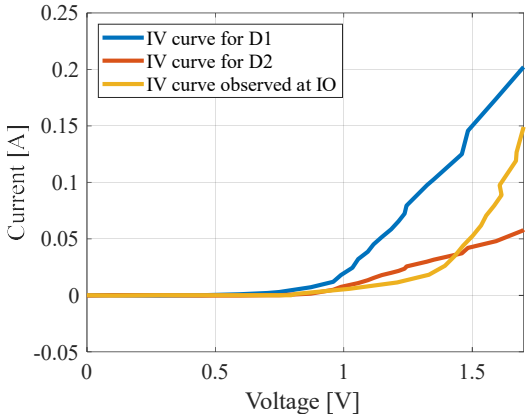


Fig 20. Extracted IV curve for single D_1 and D_2

4) The last step is to do TLP test on VDD port and model D_3 based on the tuned D_1 and D_2 to fit the measured quasi-static IV curve on VDD port.

C. Transient Response

In VF-TLP test, as discussed in single TVS modeling methodology, the shorting VDD-VSS operation is no longer effective because the pulse is too short. Any current measurement method on the VDD-VSS trace will result in overlapped reflection waveform with unpredictable time delay. Currently, there is no suitable method to de-embed the transient response from one to another, so the way to model the transient response is to start with the simplest diode, D_3, and use shorting method to characterize the rest of diodes one at a time. The conductivity modulation and the inductance will be modeled in this section. The diode before snapback and the snapback delay modulation can be modeled as well, if applicable.

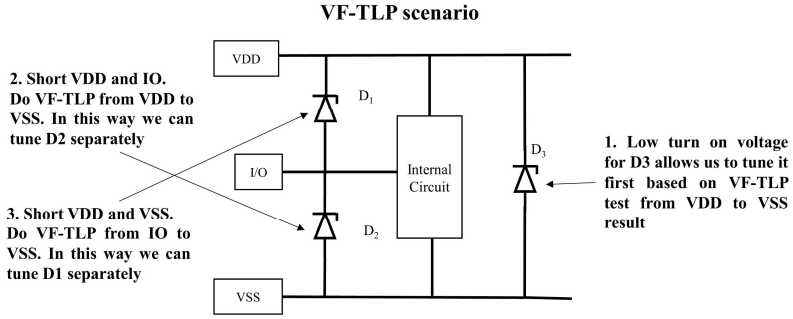
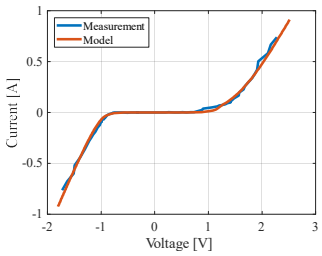


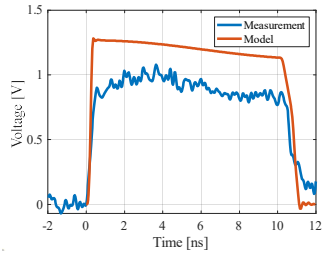
Fig 21. Under VF-TLP scenario, the flow to obtain transient waveform for different combination of

diodes. Each time short one diode and measure the transient of the other two from one port.

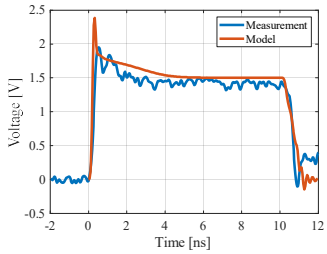
The whole process is shown in Fig. 21. First, most D_3 is likely to have low turn on voltage due to power clamp structure. Compared with other diodes, start with D_3 modeling using VF-TLP on VDD port has the minimum effect from the other paths. Once D_3 is modeled, one of the remaining two diodes can be ignored by using shorting strategy and the other remaining diode can be modeled. In this case, all three diodes can be modeled accordingly. The measured example and modeling result is shown in Fig. 22.



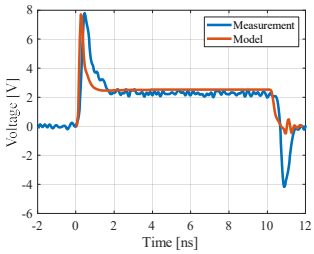
(a) Short VDD-VSS, measured IV at VDD port



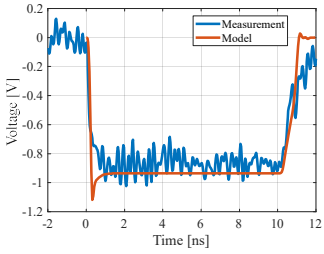
(b) Short VDD-VSS, TLP discharge at +3V



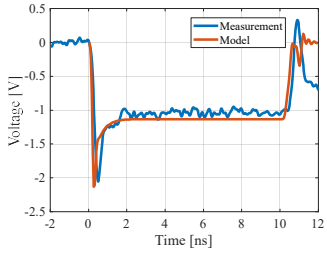
(c) Short VDD-VSS, TLP discharge at +10V



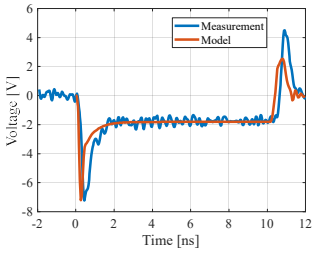
(d) Short VDD-VSS, TLP discharge at +50V



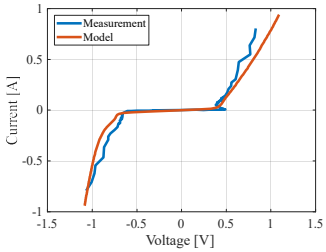
(e) Short VDD-VSS, TLP discharge at -3V



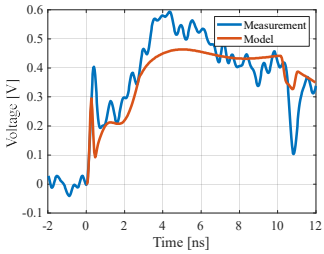
(f) Short VDD-VSS, TLP discharge at -10V



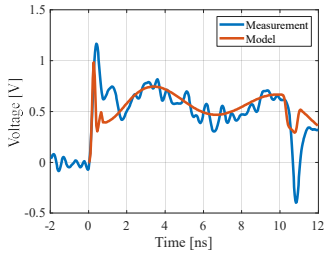
(g) Short VDD-VSS, TLP discharge at -50V



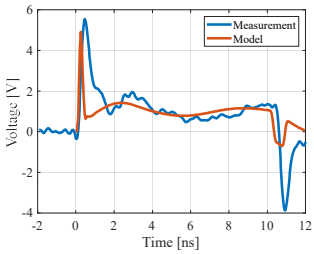
(h) Short IO-VDD, measured IV at IO port



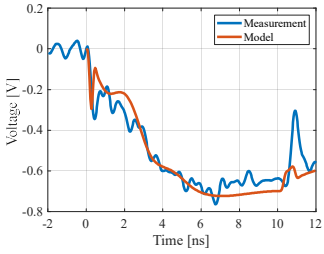
(i) Short IO-VDD, TLP discharge at +3V



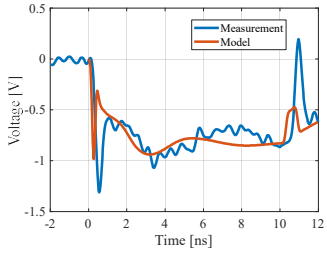
(j) Short IO-VDD, TLP discharge at +10V



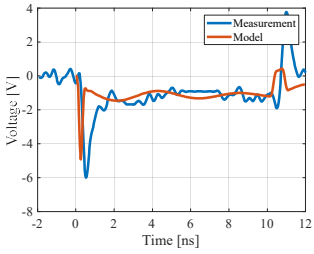
(k) Short IO-VDD, TLP discharge at +50V



(l) Short IO-VDD, TLP discharge at -3V



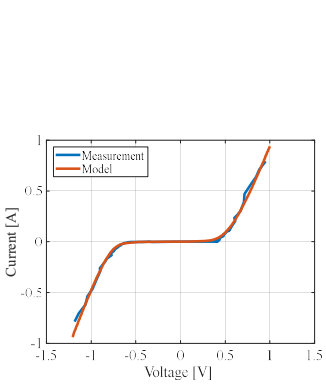
(m) Short IO-VDD, TLP discharge at -10V



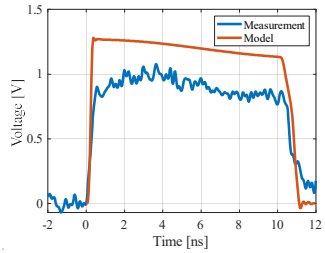
(n) Short IO-VDD, TLP discharge at -50V

Fig 22. Measurement and the simulated model for the IV curve and the corresponding transient voltage waveform at certain voltage discharge levels when shorting two pins externally.

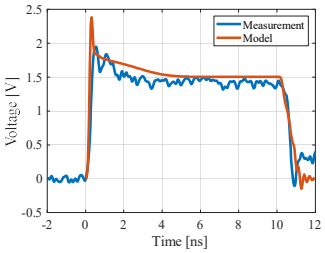
A validation is done by connecting all three diodes together and compare the measured IV curve and transient waveform result to the simulation. The result still shows comparable correlation, as shown in Fig. 23. However, due to the limitation from tuning the other two diodes, apart from D_3, the conductivity modulation of one diode can be obscured by another diode's modulation. Thus, some of the turn on time from the simulated transient response does not perfectly match the measurement. This issue may be improved in the future by using machine learning basted optimization method or reinforcement learning.



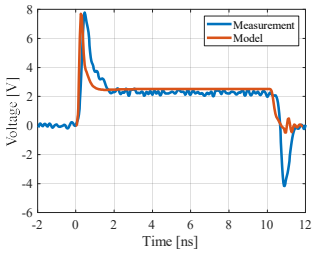
(a) All three diodes are connected, measured IV at VDD port



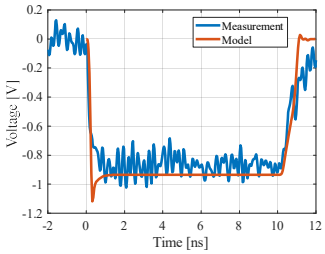
(b) TLP discharge at VDD at +3V



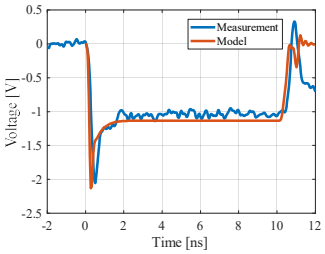
(c) TLP discharge at VDD at +10V



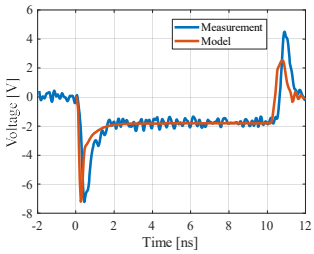
(d) TLP discharge at VDD at +50V



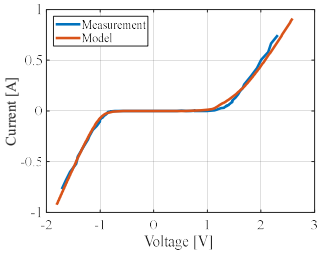
(e) TLP discharge at VDD at -3V



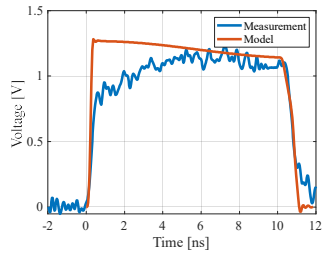
(f) TLP discharge at VDD at -10V



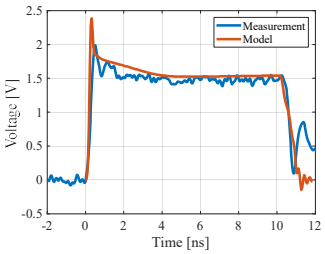
(g) TLP discharge at VDD at -50V



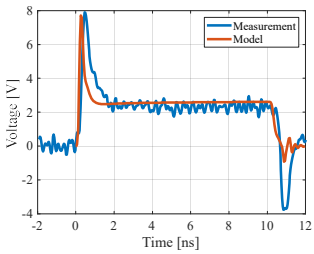
(h) All three diodes are connected, measured IV at IO port



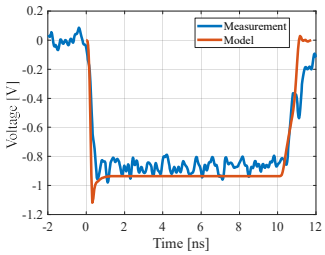
(i) TLP discharge at IO at +3V



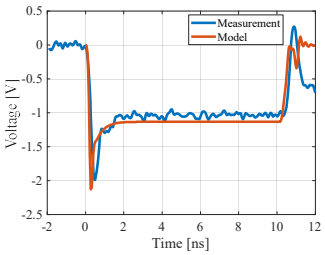
(j) TLP discharge at IO at +10V



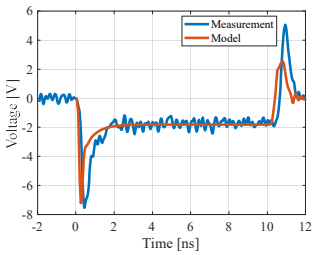
(k) TLP discharge at IO at +50V



(l) TLP discharge at IO at -3V



(m) TLP discharge at IO at -10V



(n) TLP discharge at IO at -50V

Fig 23. Measurement and model validation for the IV curve and the corresponding transient voltage waveform at certain voltage discharge levels when all three diodes are connected altogether.

Systematic Modeling Process for on-chip ESD protection structure

To characterize the ESD protection structure on an IC's peripheral IO, a systematic modeling process is proposed to model the on-chip ESD protection structures completely and accurately, as shown in Fig.24. The entire modeling process includes all the IO types discussed in the paper. For normal IO, the most important step is to determine whether the protection scheme is VSS-based or VDD-based structure, which will dictate whether three-terminal modeling methodology necessary or not. Different strategies are needed to characterize small signal model and large signal model for different types if structure. For RF IO, use of VNA to characterize the inductor based ESD protection structure is efficient. For power rail, the characterization process is similar to the general single TVS diode, while the presence of RC clamp may introduce extra circuits for ESD protection improvement, which requires further characterization.

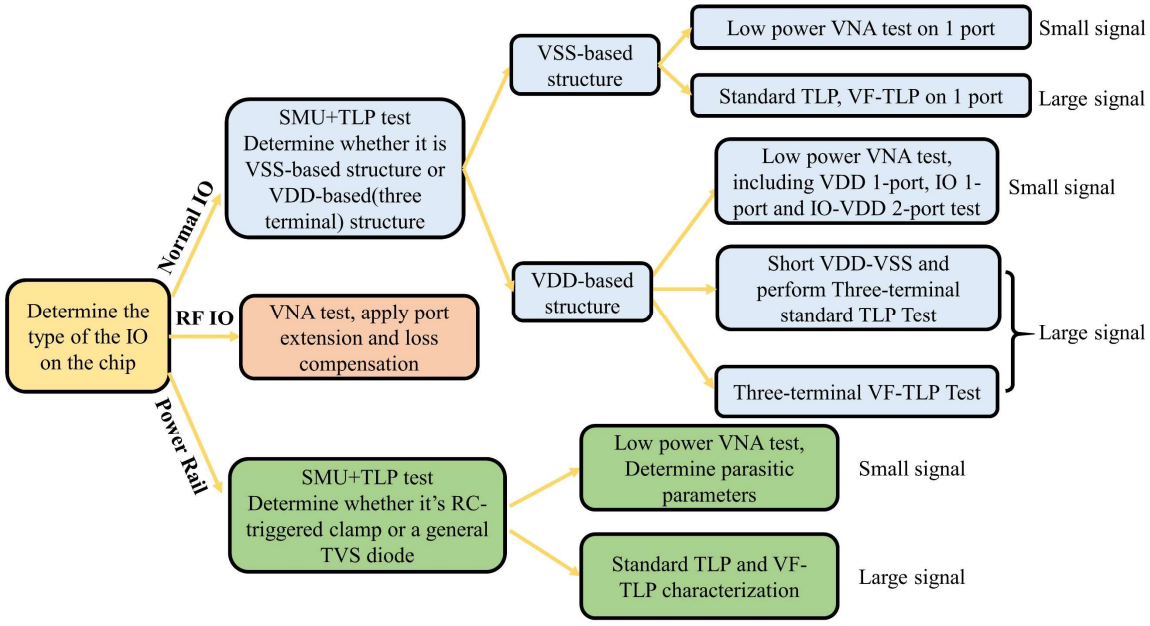


Fig 24. Systematic modeling methodology flow for on-chip ESD protection structures

Apart from the modeling procedure, there are several issues need to be clarified before finalizing the model.

1) Due to the limitation of evaluation PCB design, the three-terminal characterization methodology on quasi-static IV curve will inevitably introduce the inductance from VDD to VSS. During the modeling, this inductance is either added to D_1 or D_3. One possible way to minimize the effect is to use micro-probe directly landing on the VDD pin and VSS pin, while this increases the difficulty to find the probe with suitable pitch size. Hence, during the characterization additional inductance must also be characterized.
2) Transient waveform characterization methodology is still limited due to the lack of access to the IC pin node. In this case, extra fitting or optimization method

needs to be introduced to reduce the discrepancy. To minimize the resource of optimization with high level of accuracy, the measured VF-TLP pulse should contains three pairs: IO-VSS, VDD-VSS and IO-VDD. For IO-VDD, there should be an extra return path designed for such connection. Such optimization is the intended future work for this paper.

3) If TLP measurements at higher discharge level show small 'snapback' behavior, there could be another turned on diode or ESD protection device. However, the 'snapback' behavior can also show up at the protection device's thermal runaway point (V_{t2}). Therefore, to clearly determine what happens during the TLP measurement, SMU should be connected to the TLP test setup and test the leakage current after each TLP discharge to ensure that the device under test is still normally working.

Summary

This paper proposes a systematic modeling methodology for on-chip ESD protection structures. An overview of single TVS modeling is provided with improved compensation method. Based on the types of IOs listed as normal IO, RF IO and power rails, different types of ESD protection structures are investigated and evaluated using different methods. The three-terminal structure based on VDD-based protection strategy requires external operation to solve the linear effect on small signal part and non-linear effect on large signal part. Therefore, the new three-terminal modeling methodology is proposed based on small signal modeling, quasi-static IV curve modeling and transient response modeling. The modeling methodology provides a better match result and less modeling resource compared with general modeling strategy. Finally, a systematic modeling process is proposed for general IO port ESD protection structure characterization.

Acknowledgment

This work was supported in part by the National Science Foundation (NSF) under Grant IIP-1916535.

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