An H-Field Simulation Method to Solve Wireless Desensitization Due to the DDR Noise

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***Abstract*—Most consumer electronics nowadays integrate multi-radios and high-speed memory interfaces into a very compact form-factor. High speed digital noise is one of common aggressors for desensitization. In this paper, a comprehensive EM simulation workflow is used to analyze the coupling mechanism from the DDR power plane, and optimize the decoupling capacitor value and location to minimize the desense to the WiFi antenna. The concrete measurement has been done to prove the significant improvement with the mitigation.**

I. INTRODUCTION

In the modern-day consumer electronics products, digital noise originating from high-speed interfaces can lead to severe desense to wireless technologies [1], like Bluetooth or WiFi. Even if the clock frequency is low, the harmonics of the clock can invade radio bands (sub GHz -5G) easily. From SI/PI's perspective, the PDN analysis is used to optimize the current distribution in the power plane to minimize the noise. However, the frequency range is normally less than 100MHz and the decoupling capacitor structure is not effectively designed for high-frequency (GHz) radio bands. In the following sections, the WiFi desense caused by DDR clock noise is identified and a combined simulation and measurement workflow is presented to mitigate the issue. At last, the desense impact for various memory configurations has been shown.

II. METHODOLOGY

The presented consumer electronic product is equipped with dual band WiFi/BT and high-speed LPDDR4 chipset. The high-speed DDR clocks are routed between a solid ground plane and a DDR power plane. The 2G WiFi is heavily polluted (24dB desense worst case) by the harmonics of DDR clock. As illustrated in Fig 1, the noise aggressor is the harmonics of the DDR clock and the phase noise skirt. By using mixed-mode H-field simulation, the root-cause is found to be from the common mode noise coupling from the clock trace to the power plane. Since the least impedance of the return current path is not achieved, the noise distributes to the entire board causing high near-field coupling to the WiFi antenna. Decoupling capacitors are used to minimize the noise current loop. The values and locations are optimized through parametric sweep analysis. In this case, high frequency caps with 15pF value are used, and measurements are done for over 200 devices across 5 different DDR specifications and vendors. The results and conclusions are described in the following section.

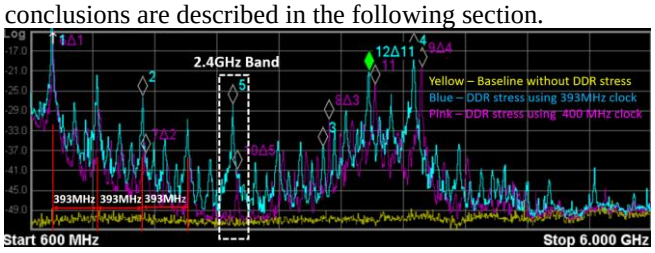

Fig1. The spectrum capture from the WiFi antenna with different DDR clock frequency settings

III. RESULTS AND CONCLUSIONS

Fig.2 depicts the common-mode H-field simulation at 2.4G that demonstrates the coupling strength from the DDR clock to the power plane. The reduced coupling after adding the decoupling capacitors as shown in Fig 2(b) can be correlated with increased isolation from the noise source to the WiFi antenna. With the de-coupling cap solution, the absolute value of isolation to WiFi antenna is increased from 65dB to 73dB.

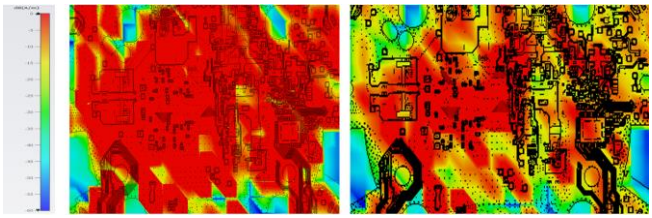

Fig 2. The H-field simulation using WiFi antenna (a) without the de-coupling caps. (b) with the de-coupling caps.

Moreover, there are 5 DDR chipsets used in this work with different memory sizes and vendors. As shown in Table I, before proper decoupling caps deployment, the devices with 512MB DDR have more desense as compared to 1GB memory banks from the same vendor. This is due to the higher capacitive loading and corresponding lower slew rate associated with the package design of the 1 GB bank. After the mitigation is applied, the WiFi desense almost gets eliminated across all the DDR memory configurations.

TABLE I. WIFI DESENSE COMPARISON WITH AND WITHOUT DECOUPLING CAPS

DDR Vendor	Without Solution		With 15pF Cap Solution	
	Desense measured	No. of units tested	Desense measured	No. of units tested
Vendor A 512M	13dB	40	1dB	28
Vendor A 1G	10dB	33	1dB	46
Vendor B 512M	24dB	41	1dB	49
Vendor B 1G	13dB	34	1dB	42
Vendor C 1G	18dB	47	3dB	43

This paper proposed a combined simulation and measurement-based method to identify and visualize a desense issue caused by the harmonics of the digital clocks. The DDR clock is the example given in the paper. A simulation workflow to determine the coupling mechanism, the values of the decoupling caps and the locations is also described. In addition, the efficiency and the robustness of this method and the solution has been proved by the real measurements over different DDR chip architectures.

REFERENCES

[1] H. Wang, V. Khilkevich, Y. Zhang, and J. Fan, "Estimating radio-frequency interference to an antenna due to near-field coupling using decomposition method based on reciprocity," *IEEE Trans. Electromagn. Compat., vol. 55, no. 6, pp. 1125–1131, Dec. 2013.*