Accurate Prediction and Mitigation of EMI from High-Speed Noise Sources using Full Wave Solver

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***Abstract*—Unintended Electromagnetic interference (EMI) is a common occurrence in all consumer electronics, which can often fail compliance margins of FCC and/or CE, when best practices of grounding, shielding and overall system integration are not followed. The measurement of EMI for regulatory compliance has been studied extensively and there are standard test labs which certifies for EMI. However, predicting the EMI radiation from a consumer electronic device through simulation is very challenging due to the complexities involved in modeling the device and noise source. This paper introduces a workflow for simulating one case of EMI radiation from a 208 MHz single-ended I/O clock generated from the System-on-Chip (SoC) in an electronic device. Through a full wave 3D solver, the radiated far field transfer function of the clock is obtained. Additionally, the spectral content of clock is measured in both time and frequency domain. Then the clock spectrum is combined with transfer function to predict EMI radiation envelope. The simulated results are then compared with the measured results from an FCC compliant laboratory. Based on the simulated and measured results, mitigation techniques are proposed to reduce the EMI to acceptable levels.**

Keywords—electromagnetic radiation; I/O clock; FCC/CE; 3D simulation; transfer function

I. INTRODUCTION

Electromagnetic interference (EMI) from electronic devices interferes with other electronic devices operating in their vicinity if it exceeds radiation levels governed by regulatory bodies like FCC/CE. This hinders the intended functionality of the device sometimes causing operational hazard. As a result, EMI is a critical compliance test that every consumer electronic device is required to pass as per FCC/CE standards [1]. Noise sources include ICs [2], memory chips [3], flexible cables [4], heatsinks [5], etc. In modern consumer electronic device, there is an increasing need for smaller, compact, and denser design. This often requires compromising critical grounding and shielding components which can potentially trigger EMI failures [1].

It is very important to predict and mitigate this failure in early developmental stages of the product as it becomes expensive to change the product design later and also causes delay in time to market. There has been a lot of research focusing on the measurement and debugging techniques of EMI failures. There are regulatory body approved test and certification labs which can accurately measure the radiation from any device. However, there has not been significant research conducted to predict the EMI failure accurately. This is mainly due to the complexity involved in modeling the device and the source of failure accurately.

A typical consumer electronic device includes a main logic board (MLB), accessory boards, flex cables and mechanical parts like heat sink, shield cans and connectors. The layout of PCB, assembly of mechanical components and their interaction is very important to minimize EMI failures. In this paper such a complex electronic device is considered as Device under Test (DUT). The source of failure is determined to be I/O clock from System on Chip (SoC) to a wireless connectivity chip at 208MHz through pre-compliance measurements. This paper addresses the feasibility of simulating EMI failure from the I/O clock source using a commercial full wave 3D solver. The simulated results are then compared to measurements obtained from a certified test house. A mitigation to minimize the EMI failure is also proposed.

II. EMI SIMULATION SETUP

Certification labs for EMI compliance use semi-anechoic chamber setup with a bi-log antenna at a distance of 3 meters or 10 meters away from the DUT. This is shown in Figure 1. The incident electric field in V/m is measured in the chamber and compared against the regulatory body defined mask. The DUT is mounted on a turn table and the measurement antenna is mounted on a vertically moving platform that can measure at different heights of 1m to 3m performing a 360 degree far-field radiated measurement in the azimuth and elevation planes. Since the measurements are done over 360^{o} in the far-field on both azimuth and elevation planes, the electric field intensity at the far-field, for a small dipole is given by:

$$E_\theta = j\eta \frac{kI_0 l \sin\theta}{4\pi r}\left[1 + \frac{1}{jkr} - \frac{1}{(kr)^2}\right] e^{-jkr} \qquad (1)$$

where 'r' can be taken as 3 meters depending on the chamber size [1]. Thus, the first step is to model a measurement setup in simulation where electric field can be accurately captured at a distance of 3 meters from the DUT in 360^{o} sphere.

Computer Simulation Technology (CST) from Dassault Systems is the simulation tool used in this paper. Figure 2 shows a simplified simulation bench, where the source and the far-field E-field probes are positioned. A simple dipole current segment with magnitude $0.2e^{-3}$ Am, is chosen as source for this first step to validate the simulation setup. Figure 3 shows the E-field obtained from simulating this current segment.

When computed using equation (1), at 1 GHz, with r = 3 meters, the E-field is calculated to be 0.88e-6 V/m or -121dBV/m. In comparison, the simulated E-field is about -118 dBV/m, at 1 GHz, which can be regarded as good correlation to the calculated value.

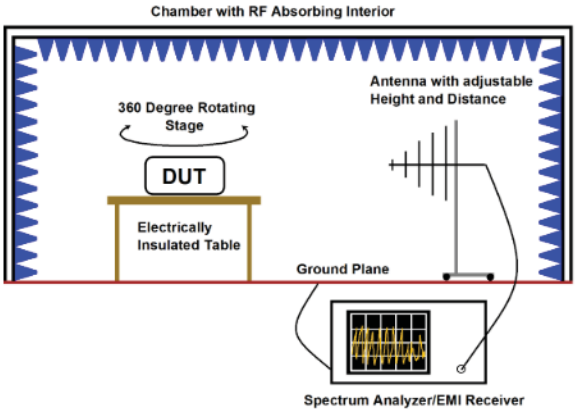

Fig. 1. Representation of EMI measurement chamber

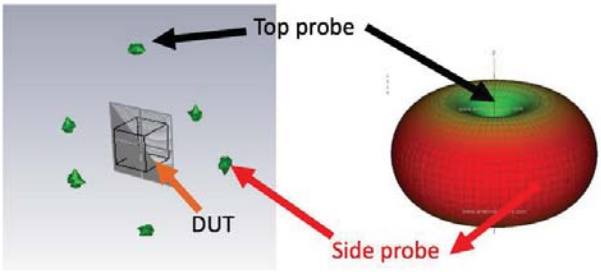

Fig. 2. *(Left)* The position of the DUT, bounding-box and a subset of the probes in the simulator *(Right)* Far-field pattern of a simple dipole antenna as an example.

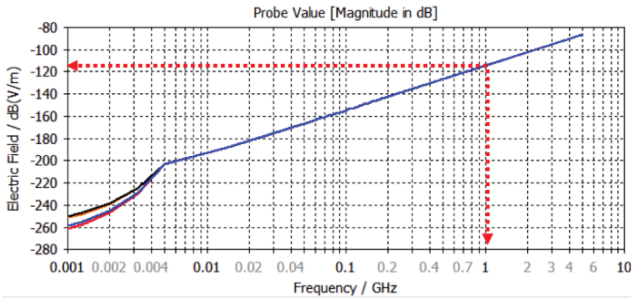

Fig. 3. Simulated E-field for a simple dipole of magnitude 0.2e-3 Am. At 1 GHz, the obtained E-field from the probes is -118 dB(V/m)). Simulated (Blue), Theoretical (Red)

In this particular example, there are 6 E-field probes (in green) that surround the bounding-box of the DUT. While only 6 probes are shown in this particular example, for the simulation a multitude of probes every 30° in azimuth and elevation can be used to improve accuracy. This will be shown in section III.

III. Proposed Workflow

The goal is to simulate EMI from the DUT like it would do in an EMI chamber. In order to achieve this, a full-scale 3D model of the device is created. All crucial elements within the model like PCBs with full layout, shield cans, heat sinks, screws etc. are retained as they play an essential role in the radiation and re-radiation mechanism. Then the EMI source is excited in the simulation using lumped port. The mode of excitation – single ended or differential is chosen based on the type of signal causing EMI failure. Then the simulation bench identified in section II is created using the DUT 3D model with the far-field E-field probes. The transfer function is defined as the ratio between the far fields over the excited power of the port. The unit of the transfer function is (V/m)/(W). The obtained transfer function from the simulation is combined with real source power level to estimate EMI levels. The term transfer function or EMI transfer function in this context is referred to the interaction between the aggressor port and the EMI probes within the sphere. Fig. 6 depicts all the curves from each probe, the peak transfer function captures the maximum radiation between the clock and the particular peak EMI probe. The workflow is then repeated with modifications to DUT model to achieve passing margin if desired. This workflow is outlined in Figure 4.

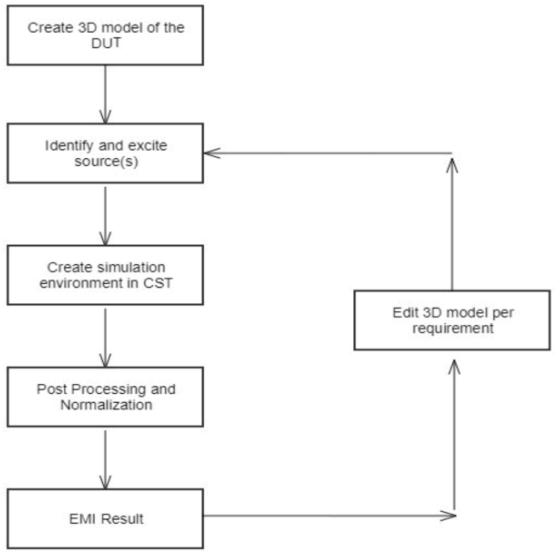

Fig. 4: EMI simulation workflow

Using the workflow, the DUT chosen is simulated in CST. Since the DUT is very complex, detailed effort has been spent to model each component accurately in 3D. As previously mentioned, the noise source is I/O clock running at 208MHz. The clock is the interface between SoC and the wireless connectivity chip. This is excited in single ended mode using lumped port. A section of DUT with I/O clock is shown in Figure 5. Mechanical components are hidden to protect the device form factor. The far field E probes are placed at every 30 degrees as shown in Figure 6.

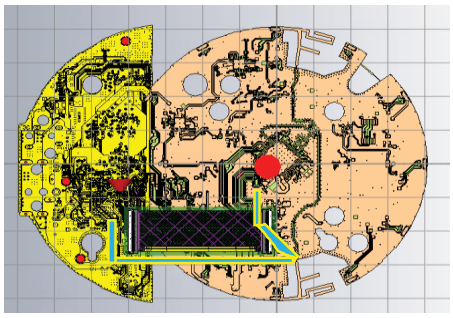

Fig. 5: PCBs of the DUT. I/O clock running from MLB (yellow) to accessory board (orange) through flex. Lumped ports and trace can be seen in red.

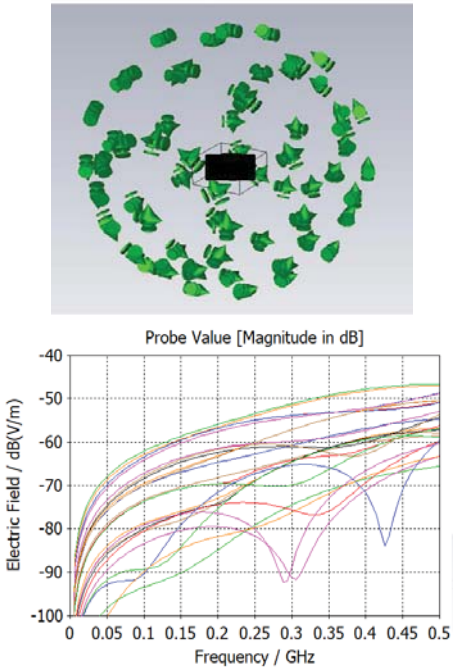

Fig. 6: (*Top)*: Simulation setup with E-field probes and DUT placed in center (*Bottom)*: E fields for different probes obtained in simulation. Each curve represents fields captured by each E-field probe.

IV. Source Measurement And Results

This section focusses on measuring the noise source spectral power for the failing frequency. From pre-compliance measurement we understand that the I/O clock is the source of failure at 208MHz. The I/O clock has test point on the PCB. Using high impedance probe the clock is measured in time domain and in the frequency domain through an FFT operation [6]. The first 3 harmonics of the clock are measured with a resolution bandwidth setting of 100 kHz. The results are shows in Figure 7. The fundamental at 208 MHz is about 6.7 dBm and the third harmonic is -17.5 dBm. This agrees with power calculated for a square wave using equation (2) where A is the peak to peak amplitude, n is the harmonic and t/T is the duty cycle.

$$c_n^+ = 2c_n = 2A\,\frac{\tau}{T}\left|\frac{\sin(n\pi\tau/T)}{n\pi\tau/T}\right|\left|\frac{\sin(n\pi\tau_r/T)}{n\pi\tau_r/T}\right| \quad for\ \ n \neq 0 \qquad (2)$$

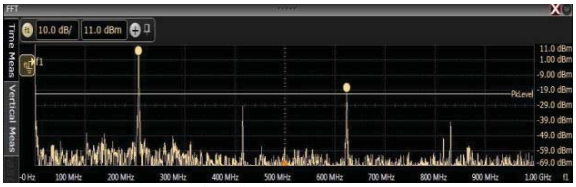

Fig. 7: Measured FFT of I/O clock EMI source. Measurement agrees with equation-based power calculation for a square wave with 50% duty cycle.

The port excitation in CST has the input power of 27dBm (0.5W) input power. In the post processing step this must be normalized to the actual source power in the real device. Another approach to getting the final field value plot is to add the EMI source and use the- 'Renorm (macro) the EMC voltage option' in CST. This would take in the transfer function and calculate the final curves based on the input data.

This calculated result from simulation is shown in Figure 8 (b). The measured result from a certified lab is also shown in Figure 8 (a) for comparison. At 208MHz the simulated EMI is 43.15dBuV/m which agrees well with measured EMI of 43.7dBuV/m. Results shows the fundamental frequency of the noise source at 208MHz is failing FCC specifications limit of 43.5dBuV/m and there is no margin.

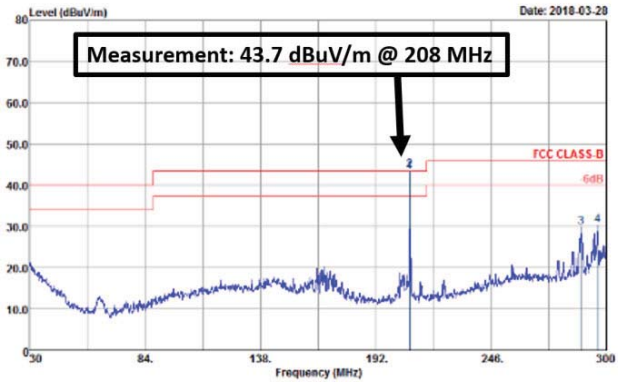

Figure 8. (a)

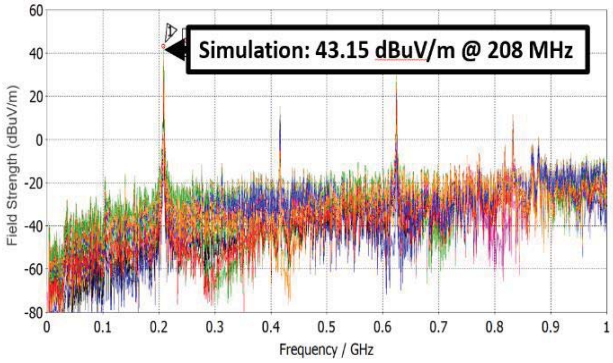

Figure 8. (b)

Fig. 8. Results at fundamental frequency f_0=208MHz; (a) Measured results from a 3m chamber from 30MHz- 300MHz; (b) Simulated results from proposed methodology highlighting the field strength at the fundamental frequency of noise

Further analysis is presented on the harmonic content of the noise source. Fig. 9 (a) shows the 3rd harmonic measurement at 624MHz is passing the FCC limit at 34dBuV/m. Fig. 9(b) shows the simulation results using the workflow and the value is 29dBuV/m at 624MHz. A difference of 5dB is observed from this comparison. Error in the 3rd harmonic could be due to error in modeling the DUT similar to the test setup in the 3m chamber. Re-measurement of the same DUT in the chamber can produce data within +/- 2dB. In addition, the noise source measured on two different devices shows a variation of 1.5dB at the third harmonic levels. This shows that the measurement and simulation uncertainty is relatively high due to real world conditions.

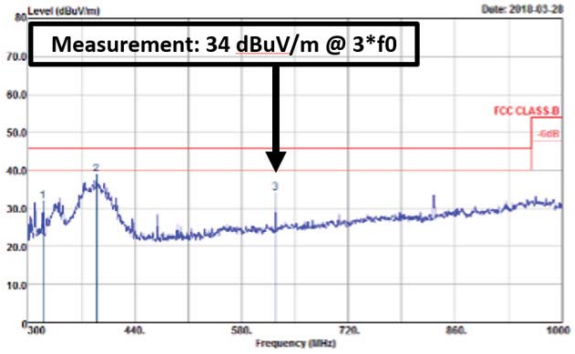

Figure 9. (a)

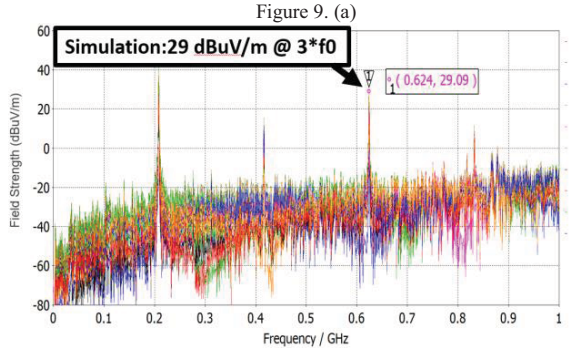

Figure 9. (b)

Fig 9. Results at third harmonic 3*f_0=624 MHz; (a): Measured results from a 3m chamber from 300MHz-1000MHz; (b): Simulated results from proposed methodology highlighting the field strength at the third harmonic

V. Mitigation Steps

As mentioned in previous sections, the I/O clock fails EMI compliance mask and there is no margin to the limits. Typically, industry requires 4dB margin to the mask. Further experiments are conducted to reduce the emissions at 208 MHz below the FCC limit. These experiments led to making grounding changes in the DUT by adding conductive foam between the heatsink and the shield can. Similar changes were mocked-up on the simulation domain and compared. Fig. 10(a) shows the results between measurement and simulation with grounding changes. The measured EMI level reduces to 36dBuV/m compared to 43.7dBuV/m on an as-is device. The simulation predicts the noise reduces to 27dBuV/m at 208MHz. Simulation is able to capture the reduction trend in EMI but the error between measurement and simulation is high in this case. Multiple factors including the modeling accuracy can cause these variations. For example, the grounding improvement in the measurements is made of conductive foam while it's simplified as a PEC block in simulation.

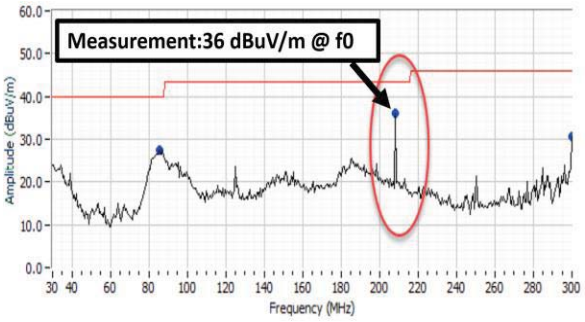

Figure 10. (a)

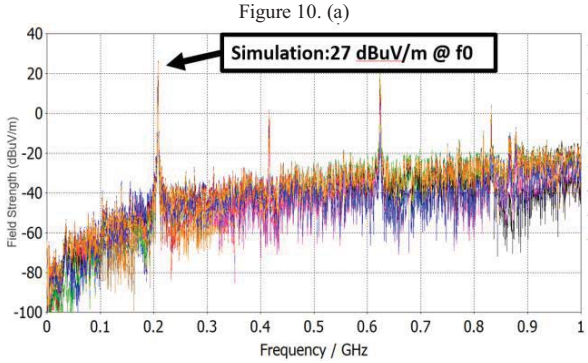

Figure 10. (b)

Fig. 10. Results at fundamental f0=208MHz from a modified DUT; (a) Measured results from a 3m chamber from 30MHz- 300MHz; (b) Simulated results from proposed workflow highlighting the reduced field strength at the fundamental.

VI. Conclusion

Previous work mostly focuses on simulations of simple DUTs or at a component level [3], [7]. This work proposes a simulation methodology for predicting EMI in a product level. In this product, the EMI from a known noise source is studied. Results obtained from the simulation are compared to the measurement. Correlation at the fundamental frequency of noise is within +/- 3dB. Bigger variation is seen while studying the 3rd harmonic emissions and possible reasons for the error are presented. Grounding improvements to reduce EMI were studied on both measurement and simulation. The proposed workflow provides a new technique to estimate EMI, reduce build cycles for consumer electronics and launch consumer electronics with a faster time to market.

References

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