Risk Reduction Strategies for SiP Design and Manufacturing

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Abstract

System-in-Package (SiP) technology provides a valuable opportunity to make products with smaller form factor, enrich functionality, and better reliability performance for consumer electronics. One key reason for SiP's success is the encapsulated structure using molding compound, which can provide protection to all the components inside and allows reduced component-to-component spacing. However, if the design or the manufacturing process have flaws, failures can also occur inside of SiP, and engineers have to spend more effort and time to conduct fault isolation, understand the root cause, and make related corrective actions. In this regard, failure risks not only occur at SiP module level. It can also happen in the final product level when assembled the SiP into it. Therefore, a comprehensive risk analysis, design and manufacturing assessment plan and an effective validation method at an early stage of the SiP development is extremely critical. This paper discusses two typical types of SiP failures. By using these two failure modes as an example, the methodology to identify and mitigate such risks early in the product development process will be demonstrated.

1. Introduction

Over the past decade, the enthusiasm over System-in-Package technology and its concept of heterogenous integration has been rapidly spreading from semiconductor community and Outsourced Semiconductor Assembly and Testing (OSAT) companies to a broader sector of the consumer electronics industry [1-5]. More and more consumer electronic companies and Original Equipment Manufacturer (OEM) companies regard SiP as the alternative solution to replace the traditional Printed Circuit Board Assembly (PCBA) based design, especially when it comes to hearable and wearable electronic products, Internet-of-Things (IoTs), and high-end portable devices. The advantages of SiP, such as miniaturization, better electrical and RF performance, and excellent reliability, is built based on a series features of this technology. For example, it leverages semiconductor manufacturing processes to realize a higher level of integration within a miniaturized form factor. It also uses thin layer metallic coating with thickness in micrometer range instead of the metal lid with thickness in millimeter range to achieve electromagnetic interference (EMI) shielding. Amongst these advanced features, the molding compound encapsulation is the most important one for SiP as it builds the foundation for all the others [5~7]. The encapsulation structure provides protections to all the components inside as well as their interconnections from the external forces and environmental hazards, such as moisture or chemical ingress. Therefore, the SiP technology can reduce the size of the solder joint area and the space between two components. The molding compound can be coated by thin layer of metallic material on its surface, mostly stainless steel and copper, to serve the function of EMI shielding. Unlike the metal lid used in PCBA, this metallic coating occupies minimal space, so the overall form factor can be significantly reduced.

However, the size shrinkage could bring a significant challenge to the SiP molding process. Defects can be covered by the molding compound, making them very difficult to be captured through normal inspection and testing process. Special techniques are required but they may still have limitations for some specific failure modes. As a consequence, sometimes the downstream OEMs have to take the risk for incoming defects. Furthermore, executing failure analysis and identifying countermeasures on SiP can be more time consuming than doing it on a PCBA product, because there is no way to quickly isolate the failure by doing the swap test since all the components are embedded underneath the molding compound. Extra processes need to be taken to expose the suspected defect location and there is always a risk to damage the original failure mode during that process. Therefore, having a comprehensive risk assessment on SiP design and manufacturing process in the early product development stage, and an effective SiP validation method that is aligned with its final application become very crucial.

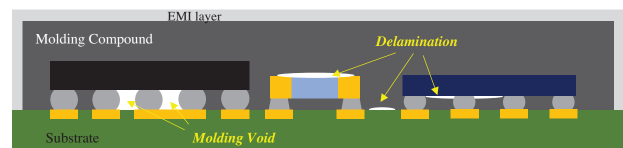


Figure 1. Schematic illustration of molding void and internal delamination inside SiP

In this paper, two typical failure modes are presented: molding voids and internal component delamination. These two failure modes are both SiP encapsulant related and share commons in the detection and the risk assessment method. Examples of these two failures inside SiP are schematically illustrated in Figure 1. Their respective failure mechanisms, contributing factors, including SiP layout design,

manufacturing process, packaging structure of IC component, and device level assembly process, are discussed in details. Failure detection method and their limitations are also included in this study.

2. Molding Void

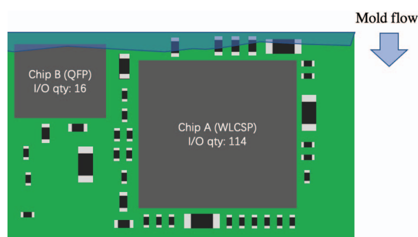
2.1. Failure Mechanism

The formation of the molding voids happens during the molding process for transfer molding technology [8]. When the liquid molding compound flows into the mold cavity, it needs to flow pass all the components and fulfill any gaps. Different flow resistance can be encountered at different locations on the SiP, which can lead to an unbalanced flow front. This unbalanced will cause air entrapment, and generate voids during the molding compound solidification process. The molding voids has become the major concern along with the SiP technology development. For instant, the component pitch size shrinks, the component-to-component spacing reduces, and the level of the heterogeneity increases as well. All of these factors are prone to make the mold flow even more unbalanced, thus leading a higher risk for molding void. Another concern is that this failure mode will cause secondary defect, such as solder extrusion, at downstream OEM factory during product assembly. Therefore, all the potential factors that can contribute to this failure need to be carefully examined at early design stage.

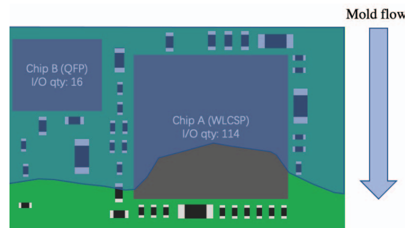
2.2. Molding Flow Analysis and Verification

The unbalanced mold flow is affected by three main factors: SiP layout, molding tool design, and the rheological behavior the molding compound [9]. For system integrators, SiP layout weighs more than the other two factors because it requires an extensive design effort. But SiP layout itself contains a lot of parameters, such as the chip size, bump size, bump pitch, component spacing, and so on. These factors interact with each other, and very difficult to be decoupled. Mold flow analysis with Computer-aided Engineering (CAE) tool is an efficiency way to assess the risk and help to optimize the SiP design [10, 11].

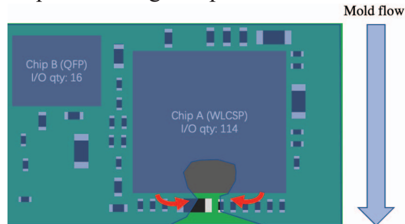
Taking the following SiP product as an example. It has a couple of major components mounted on the substrate together with a number of passives. Transfer molding process is used for encapsulation. Its layout and the progression of the molding fluid based on the mold flow simulation is schematically illustrated in Figure 2.



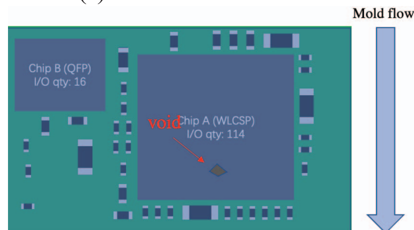
(a) Liquid molding compound starts to flow onto the SiP panel



(b) Liquid molding compound overcomes Chip A



(c) Reversed flow is created



(d) Void appears underneath Chip A component

Figure 2. Illustration of mold flow behavior

It can be seen that the mold flow is lagged behind by "Chip A"; because the melted mold flows and overcomes this component and experiences higher resistance coming from the relative larger number of the package solder balls. As a result, the molding underneath "Chip A" has the highest risk for molding void defect. In other words, Chip A has the biggest chip size and the highest number of solder bumps; these attributes provide larger resistance for the mold flow and slow down the flow speed at this area comparing with other locations on the substrate, such as area near B. Moreover, Chip A is surrounded by many passives. This will hinder the molding flow even further and cause the air more difficult to escape. The effective solution to get rid of molding voids is to redesign the SiP layout, or use different molding technology, as such compression molding, to eliminate the unbalanced mold flow induced molding voids.

It is also worthwhile to mention that the mold flow simulation result always needs to be validated by the experiment before taking the countermeasures. The procedure of the experiment is to stop the mold flow in the middle of the molding process and control the mold flow to ingress half way onto the SiP panel, so that the actual flow front can solidify before reaching the edge of the mold chassis. This semi-finished mold structure can be examined and compared with the simulation result to help improve both SiP layout design and the molding simulation Because molding void is in micro-scale and quite difficult to detect, we highly recommend to study the molding flow along with the SiP layout at design

phase. Otherwise, the molding voids induced failures analysis and the implementation of the corrective actions will consume tremendous amount of engineering effort during the manufacturing phase.

2.3. Failure Detection Methods

Scanning Acoustic Microscope (SAM) is the widely used for internal defect detection in traditional IC packaging. The advantage of SAM is that it is an efficient and non-destructive testing, which can be a good tool for both failure analysis and in-line quality monitoring. However, SAM has limitations when it is used for molding void detection in SiP module. During the operation of SAM, transducers with appropriate ultrasonic frequency need to be selected. Normally 15MHz to 50MHz are used for transmission scanning (T-mode), and 50 MHz to 230 MHz can be used for planar layer scanning (C-mode). If frequency gets higher, the image resolution can get better, but the penetration capability of the signal will get worse. It is hard to achieve both high resolution and deep penetration at the same time. Unfortunately, for SiP module, the size of molding voids can be quite small (in range of 200μm~300μm), and its thickness can be very large, especially for dual side molded structure. This makes molding void very difficult to be detected by SAM.

X-ray is another non-destructive inspection method. Although it cannot directly inspect molding void, in some cases, it still can be used to detect secondary defect that is induced by molding void, such as solder bridge. This is because when a pre-exiting void appears around a solder bump, and there is high temperature process that can let the solder re-melt, the inner pressure will push the melted solder penetrating into the void and cause solder extrusion. If the extrusion gets large enough for X-ray to detect, X-ray can indirectly identify the molding void's location via solder extrusion. However, if the solder extrusion is not big enough and will not be detectable by X-ray, it leads to unexpected escape, too.

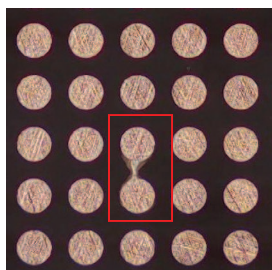


Figure 3. The molding compound under "Chip A" component after p-lapping (red box highlighted voids location between two adjacent solder balls)

Cross-section and parallel lapping (p-lapping) are two destructive methods to get the defect including molding void exposed for in-depth study. Comparing with cross-section, parallel lapping is more useful from risk assessment standing point because it does not require a pre-defined cross-sectioning location, and it can provide direct observation on the void itself and reveal critical information such as the void size and the void location, which can help engineers to decide the meaningful next steps to solve the molding void problem. Figure 3 is an example of the molding void underneath a WLCSP component after p-lapping. It is highly recommended to conduct p-lapping study when the first batch of engineering samples is available, and samples at different locations from the SiP panel should be investigated to understand if there is any location dependency on the molding void defect.

3. Internal Delamination

Delamination is another type of common failure mode that have been observed in most of traditional plastic packages. The failure mechanisms have been well studied over the past decades [12-14]. However, there are minimal reports for this failure mode in SiP module. In this paper, two different types of delamination are presented and their failure mechanism are discussed.

3.1. Component Internal Delamination

The first type of delamination failure can be inside an Integrated Circuit (IC) component inside of a SiP. In this SiP example we have components mounted both inside and outside of the molding compounds, and components are also mounted on both top side and bottom side. This results in SiP going through multiple reflow processes. This particular IC is mounted during the very first reflow process and encapsulated by transfer molding process; as a result, it has to go through all remaining reflow process multiple times. A simplified manufacturing process flow is demonstrated in Figure 4, as those processes irrelevant to this topic, such as laser marking and sputtering, are not shown here. Through T-SAM inspection, small area of delamination was detected in the center area of this component after molding process, and it propagated to a bigger area after second reflow.

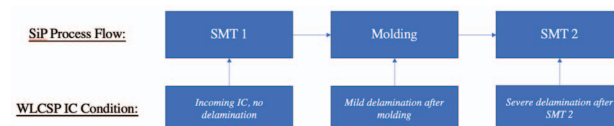


Figure 4. Process flow of SiP module

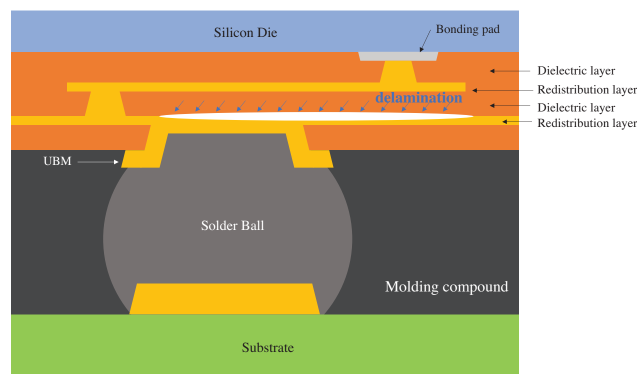


Figure 5. Delamination inside a SiP product

Cross-section result shows that the delamination is located inside the package, at the interface between the dielectric layer and the metal layer, as shown by Figure 5. it's the failure mechanism is that, the dielectric material absorbs moisture

and gets saturated under room environment. When this IC experiences a high temperature process such as molding or reflow, the moisture will evaporate. A moisture evaporation pressure was created inside the chip when its releasing path was blocked by the molding compound or uninterrupted copper region in redistribution layers (RDLs). If the RDL structure was not properly designed, it will result a pressure concentration area or even delamination when the pressure exceeded the bonding force between layers.

Comparing with other components inside of the same SiP with similar packaging structure, we noticed that the metal layer count and the dielectric material also play important roles on the delamination failure mode. The failed IC uses a different type of polymeric material for its dielectric layer, and this material has lower curing temperature and demonstrate different mechanical behavior properties. When the bonding force between molding compound and the dielectric material becomes larger than the bonding force between the metal layer and the dielectric material, the delamniaiton can occure and tear the dielectric away from the inner metal layer. However, the interaction mechanism between the molding compound and dielectric layer of the IC component is still not yet fully understood, more data needs to be collected from different package configrations.

One lesson learned from this failure is that, unless the component's datasheet specifies no encapsulation around it (like some sensors or Micro Electro Mechanical System devices), OSAT companies usually assume a low risk to encapsulate the component in SiP process. Very few component suppliers put SiP application into their consideration when they qualify the individual component because SiP is an emerging technology even though it grew very fast over the past decade. But the stress created around the component when it is encapsulated by molding compound is obviously different from that when it is mounted onto PCBA. Therefore, all components used in SiP need to be examined carefully to avoid the encapsulation induced defect. A long-term goal is to establish an industrial standard to qualify the component for SiP application.

3.2. Final Product Assembly Induced Delamination

Comparing with other traditional IC packages, SiP module offers more ways to be connected with peripheral components and to be assembled into the final consumer electrics product than the traditional surface mount process. For example, Anisotropic Conductive Film (ACF) bonding, hot bar soldering, or even mechanical assembly. However, if the SiP module does not take the final product assembly process into consideration, internal defect can also be created under certain circumstances. The following case study shows an example where a SiP module needs to be connected with a Flexible Printed Circuit (FPC) board using hot bar soldering. As demonstrated in Figure 6, this SiP module needs to be placed into a holder with its non-molded side facing up given that the SiP is single side molded. After the bonding pads on both the FPC and the SiP module getting aligned, the heated hot bar head, presses the flex onto the SiP with loading force and make the bonding between FPC and SiP. The failure was found after hot bar assembly process by electrical testing triggered by abnormal leakage current. 3D X-ray scanning revealed that delamination happened at the interface between the molding compound and the sidewall of a multi-layer ceramic capacitor (MLCC) which was located right underneath the hot bar bonding pad.

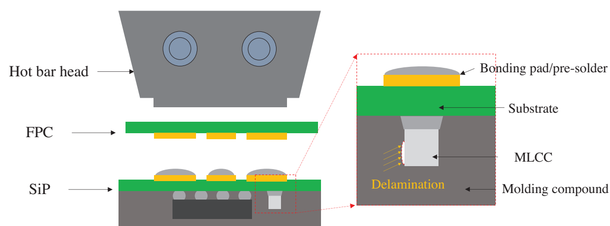


Figure 6. Top view of the SiP molded side

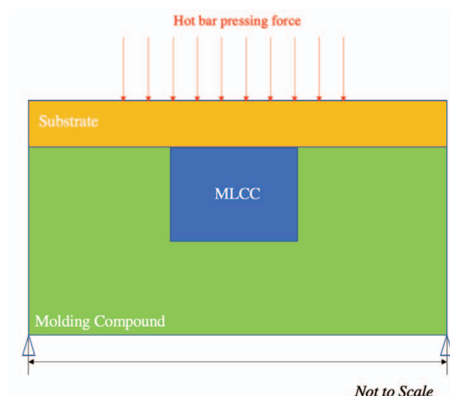


Figure 7. 2D model to simulate MLCC/molding compound delamination

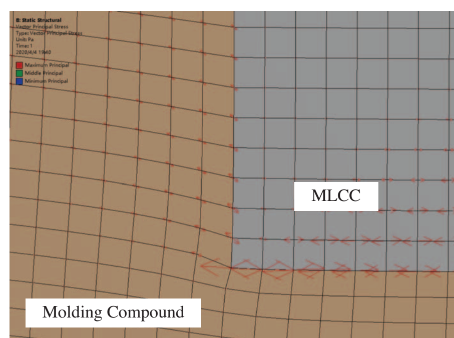


Figure 8. Stress distribution (1st principal stress)

Suspicion comes quite naturally that this delamination is caused by the pressing force during the hot bar bonding process. A simplified 2-dimensional Finite Element Model (FEM) was built and the stress distribution around the capacitor was analyzed. The simulation result suggests that when the pressing force is applied onto the SiP, the molding compound exhibits a larger amount of deformation away from the MLCC. The 1st principal stress along the interface between MLCC and molding compound tends to separate them, and the location of the maximum value also coincides with the location where the delamination happens detect from failure analysis. As a quick conclusion, even through the incoming SiP itself could be defect-free, we need to assess the final product assembly process as it can also induce possible

delamination between molding and inner passive components through thermal related process.

The learning from this case on a broader scope is that the SiP associated connection or assembly process at OEM factory needs to be included in the consideration of SiP design as well, especially when there are high temperature or high mechanical force involved in that process. For example, designing a keep-out zone for the hot bar area should be able to eliminate the risk for the abovementioned failure. This requires collaborative effort between the SiP manufacturer and system integrators. On the other hand, post-assembly SiPs should be carefully inspected to check if they are still intact inside.

4. Risk Mitigation Strategy for Molding Void and Delamination

As mentioned above, the SiP encapsulation related defects are difficult to be detected and any event of failure will require extensive effort to identify root cause and implement the related corrective actions in place. Therefore, it is very critical to assess the SiP manufacture related risk at early stage of the product development process, and carefully validate if the outcome meets the desired result. Table 1 shows suggested risk criterion and the corresponding actions aiming at the different failure modes of SiP molding void and internal delamination.

Table 1. Risk mitigation strategy for molding void and delamination

Manufacturing sector	Risk criterion	Risk mitigation action
Component level	IC with low Tg dielectric material and over-molded in the SiP process (for delam risk)	**Component sourcing stage** • Survey if any other packaging type available, such as flip chip, bare die **SiP design stage** • Survey the packaging structure, such as dielectric material • Minimize the time of reflow **First engineering sample available** • T-SAM/Cross-section inspection
SiP level	Transfer molding is used (for void risk)	**SiP design stage** • Molding flow analysis **First engineering sample available** • Conducting experiment (such as half mold) to verify with mold flow analysis • T-SAM/P-lapping inspection • X-ray inspection for secondary defect (solder extrusion)
Product level	SiP related high temperature/high pressure process in the final product assembly (for delam risk)	**SiP design stage** • Evaluation the keep-out zone of there is local heating process **First engineering sample available** • CT scan/cross-section inspection

In addition, the advanced design rule for SiP layout shall be carefully reviewed before applied with the consideration of SiP manufacturing process. For example, for fine pitch component (<0.4mm) and WLCSP component used for SiP with double side molding design, the compression molding technology shall be selected over the transform molding technology.

5. Conclusions

Voids and delamination are two typical failure modes that occurs inside SiP if SiP design and manufacturing process is not properly assessed. These two defects are difficult to detect via normal inspection or screening methods and thus are prone to escape to downstream OEM factories. Therefore, their contributing factors need to be carefully reviewed at early development stage to assess the risk and make effective countermeasures to minimize the voids and the delamination impact.

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